2017 - 2018 VLSI IEEE FINAL YEAR Projects

Project Code	IEEE 2017-18 VLSI Project Titles	Lang/Year
S301	A 2.5-ps Bin Size and 6.7-ps Resolution FPGA Time-to-Digital Converter Based on Delay Wrapping and Averaging	VLSI/2017
S302	Coordinate Rotation-Based Low Complexity K-Means Clustering Architecture	VLSI/2017
S303	Low-Power Scan-Based Built-In Self-Test Based on Weighted Pseudorandom Test Pattern Generation and Reseeding	VLSI/2017
S304	A Way-Filtering-Based Dynamic Logical–Associative Cache Architecture for Low-Energy Consumption	VLSI/2017
S305	Resource-Efficient SRAM-based Ternary Content Addressable Memory	VLSI/2017
S306	Write-Amount-Aware Management Policies for STT-RAM Caches	VLSI/2017
S307	Fault Diagnosis Schemes for Low-Energy Block Cipher Midori Benchmarked on FPGA	VLSI/2017
S308	High-Throughput and Energy-Efficient Belief Propagation Polar Code Decoder	VLSI/2017
S309	High-Speed Parallel LFSR Architectures Based on Improved State-Space Transformations	VLSI/2017
S310	Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST	VLSI/2017
S311	Stochastic Implementation and Analysis of Dynamical Systems Similar to the Logistic Map	VLSI/2017
S312	Efficient Designs of Multi-ported Memory on FPGA	VLSI/2017
S313	High-Speed and Low-Latency ECC Processor Implementation Over GF(2m) on FPGA	VLSI/2017
S314	An On-Chip Monitoring Circuit for Signal-Integrity Analysis of 8-Gb/s Chip-to-Chip Interfaces With Source-Synchronous Clock	VLSI/2017
S315	A 2.4–3.6-GHz Wideband Sub-harmonically Injection-Locked PLL with Adaptive Injection Timing Alignment Technique	VLSI/2017
S316	Hardware-Efficient Built-In Redundancy Analysis for Memory With Various Spares	VLSI/2017

S317	Fast Automatic Frequency Calibrator Using an Adaptive Frequency Search Algorithm	VLSI/2017
S318	A High-Efficiency 6.78-MHz Full Active Rectifier with Adaptive Time Delay Control for Wireless Power Transmission	VLSI/2017
S319	Scalable Device Array for Statistical Characterization of BTI-Related Parameters	VLSI/2017
S320	VLSI Design of 64bit × 64bit High Performance Multiplier with Redundant Binary Encoding	VLSI/2017
S321	ENFIRE: A Spatio-Temporal Fine-Grained Reconfigurable Hardware	VLSI/2017
S322	Hybrid Hardware/Software Floating-Point Implementations for Optimized Area and Throughput Tradeoffs	VLSI/2017
S323	Efficient Soft Cancelation Decoder Architectures for Polar Codes	VLSI/2017
S324	Low-Complexity Digit-Serial Multiplier Over GF(2m) Based on Efficient Toeplitz Block Toeplitz Matrix–Vector Product Decomposition	VLSI/2017
S325	Sign-Magnitude Encoding for Efficient VLSI Realization of Decimal Multiplication	VLSI/2017
S326	FPGA Realization of Low Register Systolic All-One-Polynomial Multipliers over GF (2m) and Their Applications in Trinomial Multipliers	VLSI/2017
S327	Low-Complexity Transformed Encoder Architectures for Quasi-Cyclic Non-binary LDPC Codes Over Subfields	VLSI/2017
S328	Antiwear Leveling Design for SSDs With Hybrid ECC Capability	VLSI/2017
S329	Energy-Efficient VLSI Realization of Binary64 Division with Redundant Number Systems	VLSI/2017
S330	A Dual-Clock VLSI Design of H.265 Sample Adaptive Offset Estimation for 8k Ultra-HD TV Encoding	VLSI/2017
S331	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing	VLSI/2017
S332	Energy-Efficient Reduce-and-Rank Using Input-Adaptive Approximations	VLSI/2017
S333	Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers	VLSI/2017
S334	An FPGA-Based Hardware Accelerator for Traffic Sign Detection	VLSI/2017

S335	Soft Error Rate Reduction of Combinational Circuits Using Gate Sizing in the Presence of Process Variations	VLSI/2017
S336	Time-Encoded Values for Highly Efficient Stochastic Circuits	VLSI/2017
S337	Design of Power and Area Efficient Approximate Multipliers	VLSI/2017
S338	COMEDI: Combinatorial Election of Diagnostic Vectors From Detection Test Sets for Logic Circuits	VLSI/2017
S339	Reordering Tests for Efficient Fail Data Collection and Tester Time Reduction	VLSI/2017
S340	Multicast-Aware High-Performance Wireless Network-on-Chip Architectures	VLSI/2017
S341	Temporarily Fine-Grained Sleep Technique for Near- and Sub-threshold Parallel Architectures	VLSI/2017
S342	Low-Power Design for a Digit-Serial Polynomial Basis Finite Field Multiplier Using Factoring Technique	VLSI/2017
S343	10T SRAM Using Half-VDD Precharge and Row-Wise Dynamically Powered Read Port for Low Switching Power and Ultralow RBL Leakage	VLSI/2017
S344	Delay Analysis for Current Mode Threshold Logic Gate Designs	VLSI/2017
S345	Area and Energy-Efficient Complementary Dual-Modular Redundancy Dynamic Memory for Space Applications	VLSI/2017
S346	Probability-Driven Multi-bit Flip-Flop Integration With Clock Gating	VLSI/2017
S347	A High-Speed and Power-Efficient Voltage Level Shifter for Dual-Supply Applications	VLSI/2017
S348	A 0.1–2-GHz Quadrature Correction Loop for Digital Multiphase Clock Generation Circuits in 130-nm CMOS	VLSI/2017
S349	Conditional-Boosting Flip-Flop for Near-Threshold Voltage Application	VLSI/2017
S350	An All-MOSFET Sub-1-V Voltage Reference With a−51-dB PSR up to 60 MHz	VLSI/2017
S351	A 65-nm CMOS Constant Current Source with Reduced PVT Variation	VLSI/2017

S352	**A Fault Tolerance Technique for Combinational Circuits Based on Selective-Transistor Redundancy**	**VLSI/2017**
S353	**Preweighted Linearized VCO Analog-to-Digital Converter**	**VLSI/2017**
S354	**A 100-mA, 99.11% Current Efficiency, 2-mVppRipple Digitally Controlled LDO with Active Ripple Suppression**	**VLSI/2017**
S355	**Sense Amplifier Half-Buffer (SAHB): A Low-Power High-Performance Asynchronous Logic QDI Cell Template**	**VLSI/2017**
S356	**On Micro-architectural Mechanisms for Cache Wear out Reduction**	**VLSI/2017**
S357	**Energy-Efficient TCAM Search Engine Design Using Priority-Decision in Memory Technology**	**VLSI/2017**
S358	**A 92-dB DR, 24.3-mW, 1.25-MHz BW Sigma–Delta Modulator Using Dynamically Biased Op Amp Sharing**	**VLSI/2017**
S359	**A 0.45 V 147–375 nW ECG Compression Processor With Wavelet Shrinkage and Adaptive Temporal Decimation Architectures**	**VLSI/2017**