S.No	IEEE 2020-2021 VLSI Project Titles	Domain	Year
1	A Carry Lookahead Adder Based on Hybrid CMOS-Memristor Logic Circuit	VLSI	2020
2	Optimization Design on Active Guard Ring to Improve Latch-Up Immunity of CMOS Integrated Circuits	VLSI	2020
3	A 7T-SRAM With Data-Write Technique by Capacitive Coupling	VLSI	2020
4	Adaptively Biased Output Cap-Less NMOS LDO With 19 ns Settling Time	VLSI	2020
5	A 60GHz CMOS Power Amplifier with Parametric Matching Networks-(ADS Software)	VLSI	2020
6	A CMOS PUF Circuit Primitive Based on a Two-Dimensional Nonlinear Dynamical System	VLSI	2020
7	A Digital-to-Time Converter with Coupled Phase- Rotating LC Oscillators in 90-nm CMOS Technology	VLSI	2020
8	A Low Noise Fault Tolerant Radiation Hardened 2.56 Gbps Clock-Data Recovery Circuit with High Speed Feed Forward Correction in 65 nm CMOS.	VLSI	
9	CMOS implementation of wide frequency bandwidth Resonator's Q-factor measurement circuit.	VLSI	2020
10	Design of Low Leakage SRAM Bitcell	VLSI	2020
11	Multistage Linear Feedback Shift Register Counters With Reduced Decoding Logic in 130-nm CMOS for Large-Scale Array Applications	VLSI	2020
12	Hybrid Logical Effort for Hybrid Logic Style Full Adders in	VLSI	2020

	Multistage Structures		
13	**A 1.2-V 2.41-GHz Three-Stage CMOS OTA With Efficient Frequency Compensation Technique**	**VLSI**	**2020**
14	**Robust Proportionate Adaptive Filter Architectures Under Impulsive Noise**	**VLSI**	**2020**
15	**Dual-Channel Multiplier for Piecewise-Polynomial Function Evaluation for Low-Power 3 D Graphics**	**VLSI**	**2020**
16	**A Two-Speed, Radix-4, Serial–Parallel Multiplier**	**VLSI**	**2020**
17	**Designing Efficient Circuits Designing Efficient Circuits Based on Runtime-Reconfigurable Field-Effect Transistors**	**VLSI**	**2020**
18	**Three-Dimensional Monolithic FinFET-Based 8T SRAM Cell Design for Enhanced Read Time and Low Leakage**	**VLSI**	**2020**
19	**Efficiently Mapping VLSI Circuits With Simple Cells**	**VLSI**	**2020**