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A Wideband Low-Noise Variable-Gain Amplifier with a 3.4 dB NF and up to 45 dB gain tuning range in 130 nm CMOS

Filipe Dias Baumgratz, *Member, IEEE,* Carlos Saavedra, *Senior Member, IEEE,* Michiel Steyaert, *Fellow, IEEE,* Filip Tavernier, *Member, IEEE,* and Sergio Bampi, *Senior Member, IEEE*

***Abstract*—A 130 nm CMOS wideband (0.2 to 3.3 GHz) low-noise variable-gain amplifier (LNVGA) with two active baluns working for phase cancellation is presented herein. The LNVGA aims for a wide gain tuning range which avoids signal compression, while enabling a low noise figure. This figure is kept low by the first stage of the LNVGA, whereas the second stage provides the gain variation. The second stage is able to deliver a wide gain tuning range thanks to the utilization of the phase cancellation technique, which is implemented by two active baluns. Since the phase cancellation technique strongly relies on the balun output balancing, a low-imbalance active balun topology is being herein proposed, analyzed in detail, designed, and tested. This new LNVGA design achieves a gain tuning range of 45 dB, a noise figure of 3.4 dB, and dissipates 19 mW in the maximum gain condition. The circuit was fabricated in 130 nm CMOS with a 1.2 V supply.**

***Index Terms*—wide gain tuning range, low noise amplifier, variable gain amplifier, phase cancellation, low-imbalance active balun**

I. Introduction

RF applications such as software-defined radio or cognitive-radio demand flexibility and programmability not only from the digital signal processing (DSP) unit but also from the RF front-end [1]. Although RF variable-gain amplifiers (VGA) are a well-known solution for that purpose, they are rarely used at RF frequencies due to the difficulty of achieving a flat gain response up to gigahertz frequencies[2].

The most straightforward methodology to vary the gain of the VGA is by controlling the bias voltage of one or more transistors of the circuit. This method achieves a low noise figure, as shown in [3], [4], in which noise figures below 4.2 dB were reported. The utilization of tunable resistive elements is another option to control the VGA gain. In fact, the resistive elements are transistors in triode operation mode which work as tunable resistors and the gain is controlled by the gate voltage of those transistors. This approach was applied in [5], achieving a 60 dB gain control range. However, this significant gain control range is only achieved thanks to multiple stages, which in turn compromise the circuit linearity. Since the transistors in triode are noisy, the noise figure of the VGA is above 16 dB, which is prohibitively high for a first stage. The last method, phase cancellation [6], uses an auxiliary path to shift the incoming signal by 180°. The primary and the phase-shifted signals are added at the output canceling each other. Despite providing a reasonable large gain tuning range, the topology proposed in [6] is unable of signal amplification. Thus, the VGA suffers from a high noise figure which compromises the receiver performance.

While the VGAs mentioned above reach either a low noise figure or a wide gain tuning range, the low-noise variable-gain amplifier in this work aims for improvement of both features simultaneously, over the wide range of 200MHz to 3.3 GHz. The low noise figure is enabled by the first stage which uses noise cancellation to reach a wideband low noise figure. The gain is controlled in the second stage, in which phase cancellation is applied so that the circuit achieves a significant gain tuning range in a single VGA. Since the second stage requires a small output imbalance, a small-imbalance active balun has been developed in this work.

This paper is organized as follows. Section II describes the main characteristics of the proposed and designed circuit. Sections III shows the simulation results and the measurement results of the fabricated circuit, respectively. Finally, Section IV summarizes the contribution of this paper.

II. Design of the proposed LNVGA

Two stages compose the LNVGA, as shown in Fig. 1. The low noise amplifier (LNA) is the first stage that aims to provide a low noise figure (NF), an average voltage gain (A_v) and the input matching to a 50 Ω signal source. The variable-voltage attenuator (VVA), the second stage, controls the gain and limits the LNVGA linearity. By controlling the gain, the LNVGA can increase the sensitivity when receiving a weak signal, whereas it avoids the signal compression when the received signal is too strong. Thus, the dynamic range of the LNVGA is enhanced.

The LNA uses a noise-cancelling topology [7], [8] that provides a low noise figure and input matching in a wide band. Since the noise-cancelling requires a secondary path to cancel the noise, the power consumption is higher than conventional LNAs. The utilization of g_m-boosting [4], [9] at M1 mitigates this drawback, for the transconductance of M1 can be reduced.

The power consumption can also be reduced by biasing the transistors in weak inversion (WI). However, the circuit bandwidth is reduced due to the size of the transistors in WI.

F. Baumgratz is with Federal University of Rio Grande do Sul, Brazil (email: fdbaumgratz@inf.ufrgs.br).
C. Saavedra is with Queen's University, Canada.
F. Tavernier and M. Steyaert are with KU Leuven, Belgium.
S. Bampi is with Federal University of Rio Grande do Sul, Brazil.

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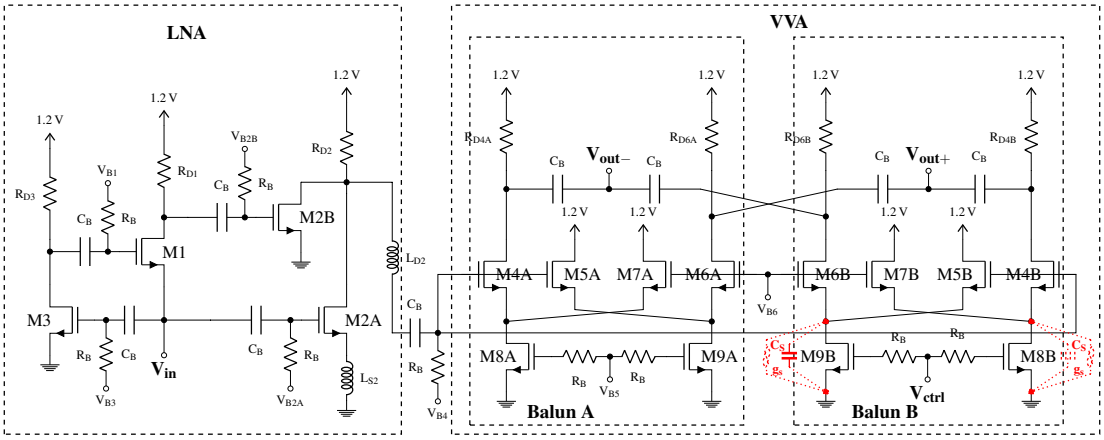

Fig. 1. The schematics of the proposed LNVGA.

This compromise between bandwidth and power consumption can be broken by using inductors or distributed amplifiers, but the former increases the circuit area and the latter degrades linearity. Thus, the LNVGA design we propose uses two inductors and transistors in moderate inversion (MI), for the best compromise between power, bandwidth, and area. Biasing the transistors in MI also offers another advantages such as a low noise [10] and a good linearity [11].

The noise-cancelling cancels both the noise and the nonlinear terms of the transistor [7]. Since M1 and M3 are in the cancellation loop, their contribution to noise and nonlinearity is reduced. Hence, the noise and nonlinearity of M2A and M2B are predominant. The noise-canceling cancels both the noise and the nonlinear terms of the transistor [7]. Since M1 and M3 are in the cancellation loop, their contribution to noise and nonlinearity is reduced. Hence, the noise and nonlinearity of M2A and M2B are predominant. Since the signal is amplified by M1 and M3 before M2B, the noise contribution of M2B becomes negligible, and M2A remains as the main noise contributor. However, this signal amplification before M2B can hinder the linearity of the circuit if M2B is not adequately sized. Therefore, we conclude that M2A limits the noise figure, while M2B affects linearity the most.

The LNVGA is single-to-differential owing to the need of out-of-phase signals to implement the phase cancellation and to easily integrate with a differential mixer. The VVA uses a common-source transistor at the input, so its input impedance is much higher than the output impedance of the LNA, which maximizes the voltage gain. Two active baluns compose the VVA, as shown in Fig. 1. Their output terminals are cross-connected, so the out-of-phase signals are added at the output node, which implements the phase cancellation [6]. The LNVGA obtains the maximum gain when the balun A is off, and the balun B is on. Meanwhile, by fully turning on both baluns, the gain of the LNVGA is minimized, for the signals are canceled at the output node. Since the phase cancellation strongly relies on the signal output imbalance of the balun, a cross-connected pair of transistors (M5 and M7 pair in each of the baluns), which is shown in Fig. 1, has been added to the differential pair in order to reduce the output imbalance [12], [13]. Consequently, the gain tuning range of the LNVGA is enhanced.

A. Input Matching

The input impedance of the LNVGA is chiefly defined by the transconductance of M1 and the loop gain through M3. However, since M2A has been biased in MI which increases the size of the transistor, the parasitic capacitances become meaningful and worsen the input matching at high frequencies.The high-frequency input impedance equation is approximated by

$$Z_{in,LNVGA}(s) \approx \left(\frac{g_{ds1}R_{D1}+1}{G_{m1}+g_{ds1}}\right) \times \frac{C_{gs2A}L_{S2}s^2+L_{s2}g_{m2A}s+1}{C_{gs2A}L_{S2}s^2+\left[g_{m2A}L_{S2}+\left(\frac{g_{ds1}R_{D1}+1}{G_{m1}+g_{ds1}}\right)C_{gs2A}\right]s+1}, \quad (1)$$

where $G_{m1} = g_{m1}(1+g_{m3}R_{d3})$, g_{ds1} is the drain-source conductance of M1, g_{m1} is the transconductance of M1, g_{m3} is the transconductance of M3, and C_{gs2A} is the gate-source capacitance of M2A. Based on (1), the input impedance and the input reflection coefficient (S11) are evaluated, and L_{S2} in Fig. 1 has been set to 460 pH, which gives a good compromise between the noise of M2A and S11.

B. Noise Figure

The noise analysis has been separately done for the LNA and VVA, for it simplifies the analysis. After that, the overall NF is calculated with the Friis equation. Hereafter, the notation of noise factor (F) will be used. This notation is related to NF by $NF = 10\log_{10}F$.

As the LNVGA is a two stage circuit, the first stage chiefly defines the noise figure (NF), and the noise contribution of the following stages are mitigated by the gain of the first one. By using the Friis equation, the noise factor of the LNVGA is calculated as

$$F_{LNVGA} = F_{LNA} + \frac{F_{VVA}-1}{\left(\frac{R_{in,LNA}}{R_{in,LNA}+R_s}\right)^2 A_{V,LNA}^2 \frac{R_s}{R_{out,LNA}}}, \quad (2)$$

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where $R_{in,LNA}$ is the LNA input resistance, $A_{V,LNA}$ is the LNA voltage gain, and $R_{out,LNA}$ is the LNA output resistance. Thus, we will firstly focus on the noise contribution of the LNA.

The noise factor of the LNA is approximated as the sum of the noise factor of each component of the LNA. Since the noise of M1, M3, and R_{d3} are completely cancelled by setting $\frac{g_{m2A}}{g_{m2B}} = \frac{R_{d1}}{R_s}$, the noise factor of the LNA is reduced to

$$F_{LNA} = 1 + \left(\frac{\gamma}{\alpha}\right)\left(\frac{1}{g_{m2A}R_s} + \frac{g_{m2B}}{g_{m2A}^2 R_s}\right) + \left(\frac{g_{m2B}}{g_{m2A}}\right)^2 \frac{R_{d1}}{R_s} + \frac{1}{g_{m2A}^2 R_s R_{d2}}. \quad (3)$$

Additionally, the noise of M2B is reduced by the gain of $G_{m1}R_{d1}$ and the noise of the resistors are small. Therefore, M2A becomes the main noise contributor of the LNA.

The noise cancellation happens whenever the condition $\frac{g_{m2A}}{g_{m2B}} = \frac{R_{d1}}{R_s}$ is observed. However, the noise factor of M2A and M2B change for different g_{m2A}/g_{m2B} ratios. Fig. 2a presents the calculated results for the NF, where g_{m2A} and g_{m2B} are the design variables.

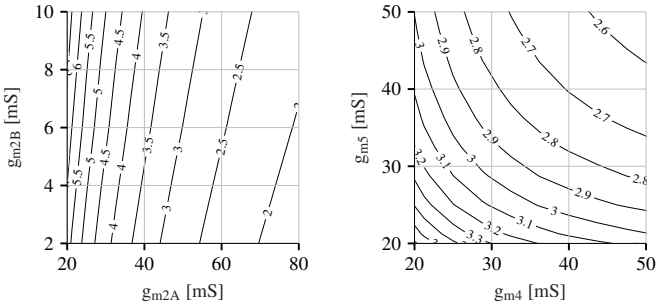

Fig. 2. The calculated NF of (a) the LNA, and (b) the LNVGA.

The values of g_{m2A} and g_{m2B} must be correctly set in such way that they minimize the NF and do not harm other design figures. For example, the size of M2A will damage the S11 at high frequency as previously discussed. Moreover, a large M2B will shift the pole at $1/R_{d1}C_{gs2B}$ to low frequencies due to the increase of C_{gs2B}. The same pole is also shifted by R_{d1}. Since g_{m2B} and R_{d1} must be proportional to each other, in order to properly cancel the noise, one could say that the transconductance g_{m2B} also shifts this pole, indirectly. Additionally, since the signal was amplified by M1 before reaching M2B, g_{m2B} reduces the LNA linearity. Finally, we chose $g_{m2A}/g_{m2B} = 14$ and $g_{m2B} = 5\ mS$. This combination yields an estimated noise figure around 2 dB and the impact on linearity is small.

Even though the gain of the LNA reduces the noise contribution of the VVA, the latter remains a high noise contributor. When the Balun B is turned off, the noise factor of the VVA is given by

$$F_{VVA} = 1 + \left(\frac{\gamma}{\alpha}\right)\left(\frac{1}{2R_S g_{m4}} + \frac{1}{2R_S g_{m5}} + \frac{g_{m8}}{2R_S g_{m5}^2}\right) + \frac{(g_{m4}+g_{m5})^2}{2R_S R_{D4} g_{m4}^2 g_{m5}^2} \quad (4)$$

respectively. These equations have been simplified thanks to the circuit symmetry. Hence, M4 = M6, M5 = M7, M8 = M9, and $R_{d4} = R_{d6}$. The impact of the VVA on the LNVGA NF is quantitatively evaluated in Fig. 2b. Even though the NF of the LNVGA can be reduced to values close to 2 dB, the linearity reduction will not worth the NF improvement. Thus, the LNVGA has been designed for an NF around 3 dB. When the Balun B is turned on, the overall NF will increase since more noise sources are included into the circuit and it works as an attenuator.

C. Voltage Gain

Similar to the NF analysis, the gain of the LNA and the VVA will be separately discussed. The interface between the LNA and the VVA is chosen for the maximum voltage gain. Hence, $R_{out,LNA} \ll R_{in,VVA}$.

The LNA transfer function is given by

$$H_{LNA}(s) \approx -\frac{C_{gs1}C_{gs2b}R_{d1}R_{d3}s^2 + (C_{gs1}R_{d3} + C_{gs2b}R_{d1})s + 2}{(C_{gs2B}R_{d1}s+1)(C_L L_{d2}s^2 + C_L R_{dout}s + 1)} \times \frac{g_{m2A}R_{dout}}{(C_{gs1}R_{d3}s+1)}, \quad (5)$$

where C_L is the input capacitance of the VVA, and R_{dout} is the parallel association of R_{d2}, g_{ds2A}, and g_{ds2B}. The circuit is considered under input matching and noise-canceling condition.

Setting the dominant pole, the inductor L_{d2} is crucial for achieving a large bandwidth and a flat gain. Although the two other poles are not dominant, they must be carefully placed so that they do not take the dominant pole position and reduce the circuit bandwidth. It is important to keep those secondary poles at frequencies much higher than that of the dominant pole. Hence, the best option is to minimize the capacitances C_{gs1} and C_{gs2B}.

The VVA is composed by two identical baluns that are presented in Fig. 1. The Balun A has a fixed gain, whereas the Balun B has a variable gain that is controlled by the voltage V_{ctrl}. When V_{ctrl} is 0 V, the Balun is turned off and the gain is maximum. By increasing V_{ctrl} the gain of the VVA drops, the gain is minimum when V_{ctrl} equals V_{b5}.

The transfer function of the VVA used in this LNVGA with the Balun B turned off is given by

$$H_{VVA}(s) \approx -\frac{\frac{g_{m4}R_{d4}(g_s+2g_{m5})}{g_s+g_{m4}+g_{m5}}\left(\frac{2C_{gs5}+C_S}{g_s+2g_{m5}}s+1\right)}{(R_{d4}C_L s+1)\left(\frac{C_{gs4}+C_{gs5}+C_S}{g_s+g_{m4}+g_{m5}}s+1\right)}, \quad (6)$$

in which g_s and C_s are the parallel parasitic conductance and capacitance, respectively, that are observed at the drain of M8 and M9 (shown in Fig. 1). In comparison with the VVA in [13], this VVA has a larger gain tuning range since its maximum gain is higher than that in [13].

The proposed active balun uses the transistors M5 and M7 to reduce the output imbalance, yet this technique only tackles the imbalance due to the parasitic components of the tail transistors (M8 and M9). The imbalance caused by C_{gd4} is neglected because it only harms the circuit at frequencies outside our band of interest. Moreover, since the load of the

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VVA does not affect the output imbalance, a generic load Y_L is considered for the imbalance analysis.

The transfer function of the positive branch of the balun needs to be equal to that of the negative branch so that the output will be balanced, i.e. the imbalance will be zero. The balun transfer functions of negative and positive branches are

$$H_{balun,n} \approx -\frac{g_{m4}(g_s+g_{m5})\left(\frac{C_{gs5}+C_S}{g_s+g_{m5}}s+1\right)}{Y_L(g_s+g_{m4}+g_{m5})\left(\frac{C_{gs4}+C_{gs5}+C_S}{g_s+g_{m4}+g_{m5}}s+1\right)} \quad (7)$$

and

$$H_{balun,p} \approx \frac{g_{m4}g_{m5}\left(\frac{C_{gs5}}{g_{m5}}s+1\right)}{Y_L(g_s+g_{m4}+g_{m5})\left(\frac{C_{gs4}+C_{gs5}+C_S}{g_s+g_{m4}+g_{m5}}s+1\right)} \quad (8)$$

respectively.

The magnitude imbalance happens because $g_{m4}(g_{m5}+g_s) \neq g_{m4}g_{m5}$, so the magnitude imbalance is reduced if $g_{m5} \gg g_s$. Since M5 and M7 do not have a resistor connected to their drains, they can have a higher current without falling into the triode region, so the g_m of M5 and M7 will be larger than those of M4 and M6 and much larger than g_s. Hence, the magnitude imbalance is reduced. The phase imbalance happens because $\frac{C_{gs5}+C_S}{g_{m5}+g_s} \neq \frac{C_{gs5}}{g_{m5}}$. Hence, the phase imbalance will be reduced if both $g_{m5} \gg g_s$ and $C_{gs5} \gg C_S$. First, instead of using one transistor at the tail, the proposed active balun uses two (M8 and M9), that reduces C_S by 50%. Additionally, M8 and M9 have been biased in strong inversion (SI) that further reduces the size of the transistors and also their capacitances.

D. Linearity

The MOSFET current can be represented by a power series on v_{gs}:

$$i_{ds} = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + \cdots \quad (9)$$

where g_1 is the transconductance (g_m), $g_2 = \frac{1}{2!}\frac{\partial^2 I_{DS}}{\partial V_{GS}^2}$, and $g_3 = \frac{1}{3!}\frac{\partial^3 I_{DS}}{\partial V_{GS}^3}$. The second order non-linearities and the third order non-linearities are represented by the second and the third element of the series respectively.

Due to the small g_3, it is common to bias the transistors in SI whenever a high linearity is needed. However, this choice leads to a high power consumption. Moreover, there are some bias points in MI that have values of g_3 smaller than that in SI. Indeed, the values of g_3 are smaller within $15 \leq {}^{g_m}/_{I_D} \leq 20$ than their values in SI, i.e., ${}^{g_m}/_{I_D} \leq 9$. There is even a bias point where $g_3 = 0$. By biasing the transistors close to this bias point, the IIP3 will be enhanced [11] in addition to reducing the power consumption. The third order distortion term can also be canceled by using two transistors biased in such way that their g_3 have an opposite polarity.

Conversely to [13], the transistors of this design are biased in MI instead of WI so that their g_3 can have an opposite polarity and be cancelled. The transistors M2A and M2B have been biased with a ${}^{g_m}/_{I_D}$ of 16.9 and 17.9 respectively, for the cancellation of g_3. The pair M4-M5 has also been biased so that their g_3 cancel each other. The transistors M1 and M3 have been both biased with a ${}^{g_m}/_{I_D}$ of 13 because their nonlinear terms are canceled in the same way as the noise, hence their linearity is not a concern. As a result, the IIP3 of this LNVGA is better than that of [13] despite its higher gain.

III. Measurement Results

The LNVGA has been fabricated in GF 130 nm CMOS. Fig. 3 shows the chip photograph and its dimensions. The core area of the chip occupies 0.15 mm^2, excluding pads area, and it is concentrated on the central region. Moreover, the circuit has been tested using probes to the RF pads but bondwires to the DC pads, which were connected to a PCB. Consequently, the LNVGA has its performance affected by those bondwires, as we are going to discuss further in this section. The simulation results had been presented in [12] and, for the sake of brevity, those results are not going to be repeated hereafter.

The power consumption remains a problem in the proposed LNVGA topology. This LNVGA consumes 19 mW when the gain is maximum and 27 mW when the gain is minimum.

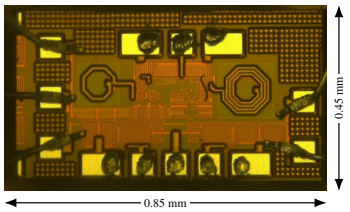

Fig. 3. Chip photograph of this LNVGA.

TABLE I
LNVGA RESULTS IN COMPARISON WITH PRIOR WORKS.

REF.	Gain [dB]	$NF_{min.}$ [dB]	IIP3 [dBm]	BW [GHz]	Power [mW]	Area [mm^2]	CMOS Process
[3]	-10∼8	4.2	1.8	0.03-7	9	1.16 [c]	180nm
[6]	-30∼-2.6	3	N/A	1-3.5	18	0.05 [c]	180nm
[5]	-10∼50	17	-45.4∼-3.4 [a]	0.01-2.2	2.5	0.01	90nm
[4]	-5∼11	3.2	-4.5∼0	1-5	19	0.067	180nm
[13]	-25∼10	4.9	-10	0.4-3.3	15.6	0.15	130nm
This work	-25∼20	3.4	-11.1 [b]	0.2-3.3	19	0.15	130nm

[a] Calculated from P1dB. [b] Simulation result. [c] Area including bond pads.

The gain tuning range of the LNVGA, in the frequency range from 200 MHz to 4 GHz, is presented in Fig. 4. The circuit has a maximum gain of 20 dB at $V_{CTRL} = 0$ V and a minimum gain of -25 dB at $V_{CTRL} = 0.8$ V. However, the gain does not remain flat at low gain levels due to the length of the GND bondwire ($\approx$ 4 mm). Despite this issue, the LNVGA still achieves a wide band, for the 3 dB cutoff frequency is 3.3 GHz at the maximum gain. The gain tuning range is 45 dB. In comparison to the LNVGA in [13], and the RF VGAs in [3], [4], [6], the LNVGA presented here shows a far superior gain tuning range.

The measurements of the input reflection coefficient (S11), shown in Fig. 5, demonstrate that, regardless of the gain, the input of the LNVGA remains matched to 50 Ω within the entire band. The GND bondwire that harms the gain flatness also affects the S11 as it is noticeable in Fig. 5, yet the S11 remains below -10 dB.

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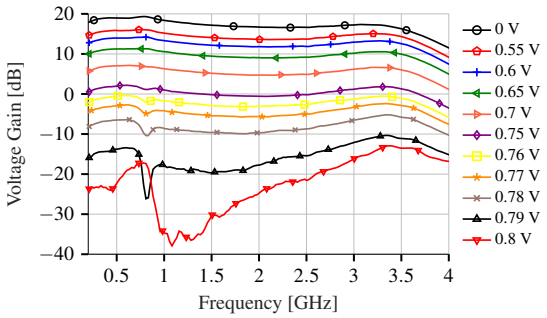

Fig. 4. Measured voltage gain variation with V_{CTRL} across the entire band.

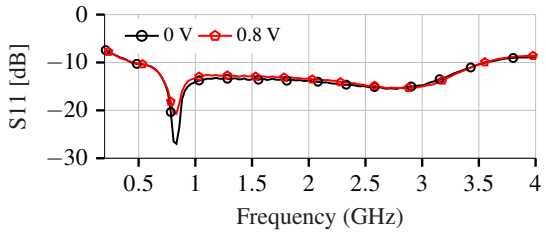

Fig. 5. S11 measured results at maximum gain and minimum gain.

In contrast to the S11, the NF considerably changes with the gain. Fig. 6 shows that the NF sharply rises as the gain falls. Although the LNA reduces the LNVGA's NF, it cannot hold the NF low after the LNVGA gain falls below zero. Hence, the NF sharply rises after this point due to the massive noise contribution of the VVA. Nevertheless, the high NF at the minimum gain is not a problem since the purpose of the minimum gain mode is to receive strong signals without compression. The LNVGA has a measured minimum NF of 3.4 dB, which is similar to the simulated results.

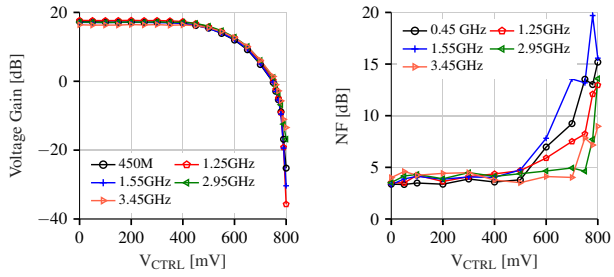

Fig. 6. The variation of the (a) voltage gain and (b) NF of the LNVGA.

A comparison with prior works is shown in Tab. I. Although the gain tuning range reported in [5] is larger than that of this LNVGA, it has not only a prohibitively high NF but also a low IIP3. In comparison to [3] and [4], this LNVGA achieves a similar NF but with a much larger gain tuning range. Unlike the other VGAs, the LNVGA is able to provide both a large gain tuning range and a low NF. Additionally, this LNVGA presented a larger gain tuning range and a lower NF than the LNVGA in [13].

IV. Conclusion

The design of a LNVGA in 130 nm CMOS with active baluns has been herein presented and analyzed in detail. Our topology achieved both a low noise figure and a wide gain tuning range within a wide band, whereas the circuits previously reported have failed to simultaneously improve both figures. Our design improves by almost 10 dB the gain tuning range and by 1.5 dB the NF of a previously reported LNVGA with active baluns [13]. The key point to improve the performance was the active balun, in which the gain and NF have been enhanced by removing the active inductors. Despite this modification, the active balun remains with a low imbalance, and the band of the LNVGA remains unchanged. This new LNVGA design achieves a gain tuning range of 45 dB and a minimum NF of 3.4 dB, while it consumes 19 mW from 1.2 V supply.

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