High-Efficiency Asymmetric Forward-Flyback Converter for Wide Output Power Range

Hyeon-Seok Lee, Hyung-Jin Choe, Seok-Hyeong Ham, and Bongkoo Kang, *Member*, *IEEE*

***Abstract*—This paper proposes an asymmetric forward-flyback dc-dc converter that has high power-conversion efficiency η_e over a wide output power range. To solve the problem of ringing in the voltage of the rectifier diodes and the problem of duty loss in the conventional asymmetric half-bridge (AHB) converter, the proposed converter uses a voltage doubler structure with a forward inductor L_f in the second stage, instead of using the transformer leakage inductance, to control output current. L_f resonates with the capacitors in the voltage doubler to achieve a zero-voltage turn-on of switches and a zero-current turn-off of diodes for a wide output power range. The proposed converter could operate at a wider input voltage range than the other AHB converters. η_e was measured as 95.9% at output power P_O = 100 W and as 90% at P_O = 10 W, when the converter was operated at input voltage 390 V, output voltage 142 V, and switching frequency 100 kHz.**

***Index Terms*—DC-DC power conversion, Resonance, Stress, Transformer windings.**

I. Introduction

The flyback converter (Fig. 1(a)) is an isolated step-down DC/DC converter that is composed only of one switch, one transformer, and one diode [1,2]. It has been used widely for an output power $P_O \leq 100$ W because of the simplicity of circuit [3]-[6]. However, the flyback converter has low power-conversion efficiency η_e at a low P_O because the switching frequency increases as P_O decreases, and its switch is subjected to high voltage stress because of the leakage inductance L_{lk1} from transformer.

The asymmetric half-bridge (AHB) converter (Fig. 1(b)) has been used in the power supplies for plasma display panels and liquid crystal displays, which require $100 \leq P_O \leq 500$ W [7]-[9], and in adapters, battery chargers, and light emitting diode (LED) lamp drivers, which require $P_O \leq 100$ W [10]-[13]. The primary stage of the AHB is similar to that of the flyback converter and the secondary stage is the same as that of the half-bridge converter [14,15]. AHB remedies the deficiencies of the flyback converter by using a switch S_2 at the primary stage, to provide a free-wheeling path for the energy stored in the transformer leakage inductance L_{lk1}. The off-state voltage of switch S_2 is clamped to the input voltage V_{IN}. AHB converter uses L_{lk1} to achieve a zero voltage switching (ZVS) turn-on of S_1 and S_2 at a fixed switching frequency, so it has high η_e. However, L_{lk1} must be high to achieve ZVS for a wide range of P_O, so the duty loss to provide a freewheeling path for the rectifier diodes D_1 and D_2 increases. An additional problem is that D_1 and D_2 suffer from a voltage ringing problem that is caused by a resonance between L_{lk1} and the parasitic capacitance of D_1 and D_2 [16]-[19].

The AHB converter with voltage doubler structure (Fig. 1(c)) has the same primary circuit as the AHB converter, but has a voltage doubler as the secondary circuit [20,21]. The voltage doubler solves the problem of voltage ringing at the secondary stage of AHB converter by clamping the voltages of D_1 and D_2 to the output voltage V_O, so the voltage stress of the diodes is reduced. Because the loss caused by the freewheeling current of D_1 and D_2 is eliminated, the AHB converter with a voltage doubler has high η_e. However, this converter has narrow range of V_{IN} for a proper operation and requires big input capacitor to secure hold-up time [22,23].

The dual-resonant converter (Fig. 1(d)), which is another converter that uses a voltage doubler in the secondary stage, achieves ZVS turn-on of switches by using magnetizing inductance L_m, instead of L_{lk1}. This converter uses an active clamp structure that consists of S_2 and C_C in the primary stage [24]-[26], and uses a resonance between the secondary leakage inductance L_{lk2} and output capacitors C_1 and C_2 to achieve zero current switching (ZCS) of the rectifier diodes D_1 and D_2, so it has high η_e. However, the voltage of C_C increases the voltage stress of switches, and the current stress of D_2 is high when the converter is operated in a discontinuous conduction mode (DCM). In addition, a transformer with $L_{lk2} < 1$ μH cannot be designed easily.

This paper proposes a dc-dc converter that uses a blocking capacitor C_B in the primary stage, instead of C_C, and a voltage doubler structure with a forward inductor L_f. The proposed converter increases the range of V_{IN} by using unbalanced secondary turns of transformer, and can reduce the voltage stress of switches and the current stress of diodes. The circuit structure and operating principles of the proposed converter are described in Section II, design considerations are given in Section III, experimental results are given in Section IV, and a

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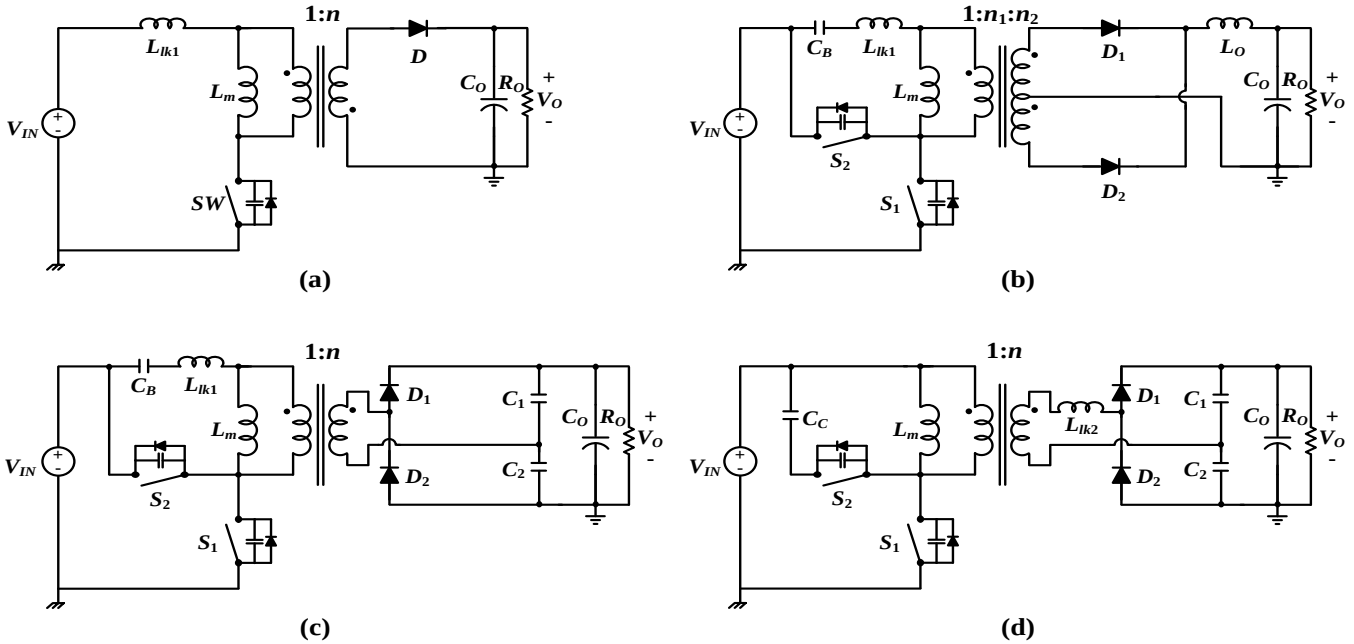

Fig. 1. Circuit structure of (a) flyback converter, (b) AHB converter, (c) AHB converter using voltage doubler, and (d) dual-resonant converter.

conclusion is given in Section V.

II. Proposed DC-DC Converter

A. Circuit Structure

The primary stage of the proposed converter (Fig. 2) is the same as that of AHB converter. The two switches S_1 and S_2 operate at different duty ratios. The secondary stage is a voltage doubler circuit with a forward inductor L_f, which helps achieve ZVS turn-on of S_1 and S_2, and acts as an output filter. The problem of the duty loss, which is observed in the AHB converter, is minimized because no freewheeling current flows through D_1 and D_2; a resonance between L_f and C_1, and C_2 achieves ZCS turn-off of diodes. Also, C_1 and C_2 remove the voltage ringing in the rectifier diodes by clamping the reverse voltage of D_1 and D_2.

B. Principle of Operation

The proposed converter operates at a fixed switching period $T_S = 1/f_S$, where f_S is switching frequency, but changes the switching duty D to control the voltage conversion ratio. The equivalent circuits (Fig. 3) and waveforms (Fig. 4) of the proposed converter were obtained under the following assumptions: 1) $D \le 50$ % for S_1, 2) D_1 and D_2 are ideal diodes, 3) all inductors and capacitors are loss free, 4) C_B is large enough, so that the voltage ripple of C_B is negligible and C_B can be represented by a constant voltage source V_{CB}, 5) C_O is large enough, so that C_O and R_O can be represented by a constant voltage V_O, 6) the leakage inductance of transformer is negligible, and 7) the turn ratio of transformer is $1 : n_1 : n_2$, where n_1 and n_2 are the turn ratios of secondary windings to the primary winding. The proposed converter operates in seven modes:

Mode 1 [Fig. 3(a), $t_0 < t < t_1$]: At $t = t_0$, S_2 is turned off and the converter enters the dead-time interval which prevents a simultaneous turn-on of S_1 and S_2. During this period, the output capacitance C_{S2} of S_2 charges from 0 V to V_{IN}, and the output capacitance C_{S1} of S_1 discharges from V_{IN} to 0 V. This mode ends when i_{D2} is gradually reduced to 0 A, thereby achieving ZCS turn-off of D_2.

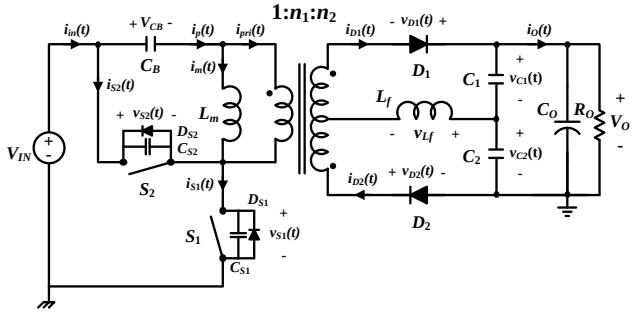

Fig. 2. Circuit structure of the proposed converter.

Mode 2 [Fig. 3(b), $t_1 < t < t_2$]: At $t = t_1$, i_m flowing through L_m remains in a negative direction for S_1, so the body-diode D_{S1} of S_1 is turned on, and S_1 is turned-on subsequently. At this time, D_1 is turned on and i_{D1} starts to flow. The dc voltage V_{CB} of C_B is obtained by applying volt-second balance for L_m as

$$V_{CB} = DV_{IN}$$

The current flowing through L_m is given by

$$i_m(t) = \frac{(1-D)V_{IN}}{L_m}(t - t_1) + i_m(t_1) \tag{1}$$

for $t_1 < t < t_4$, L_f resonates with C_1 and C_2, so i_{D1} becomes

$$i_{D1}(t) = \frac{n_1(1-D)V_{IN} - v_{C1}(t_1)}{\sqrt{L_f / (C_1 + C_2)}} \cdot \sin\left[\omega_r (t - t_1)\right] \tag{2}$$

where $\omega_r = 1/\sqrt{L_f (C_1 + C_2)}$. During this period, i_{S1} flows through D_{S1}, and is given as

$$i_{S1}(t) = i_m(t) + i_{pri}(t) = i_m(t) + n_1 \cdot i_{D1}(t).$$

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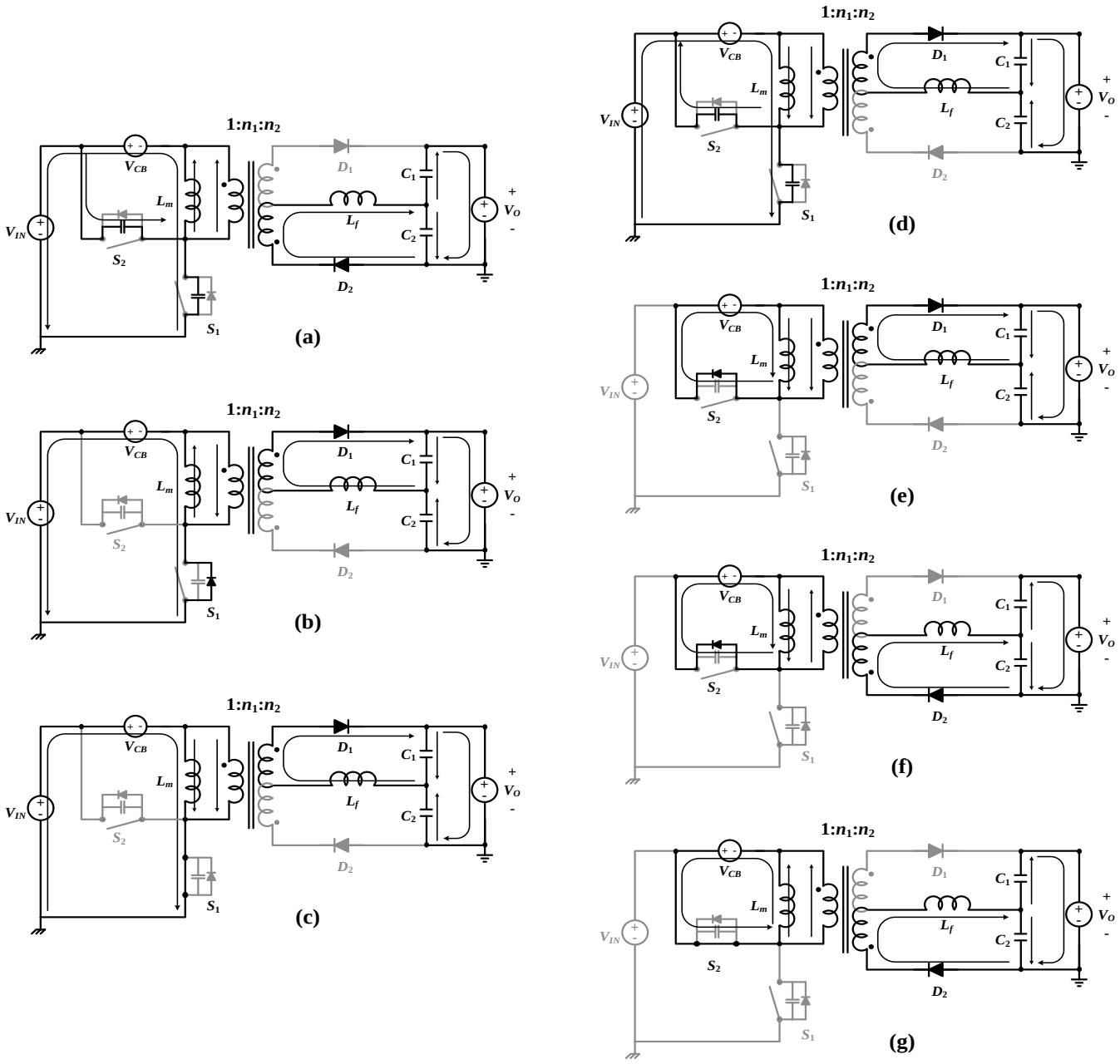


Fig. 3. Circuit diagrams for the modes of operation.

Mode 3 [Fig. 3(c), $t_2 < t < t_3$]: S_1 has been turned on before $t = t_2$, D_{S1} is turned off at $t = t_2$ when $i_m = -i_{pri}$, where i_{pri} is the current through primary winding of the ideal transformer. The same i_{D1} as (2) charges C_1; energy is transferred to the output side from input. This mode ends when S_1 is turned off.

Mode 4 [Fig. 3(d), $t_3 < t < t_4$]: At $t = t_3$, S_1 is turned off and S_2 remains in the off state, so the converter enters the dead-time interval. C_{S2} discharges from V_{IN} to 0 V and C_{S1} charges from 0 V to V_{IN}. This mode ends when the charging and discharging processes are finished.

Mode 5 [Fig. 3(e), $t_4 < t < t_5$]: i_{D1} starts to decrease at $t = t_4$, and the energy stored in L_f is transferred to C_1. For $t_4 < t < T_S + t_1$, the voltage V_{Lm} across L_m equals to $-V_{CB}$, so

$$i_m(t) = -\frac{DV_{IN}}{L_m}(t - t_4) + i_m(t_4).$$

During this period, the body-diode D_{S2} of S_2 is turned on because i_m and i_{pri} flows in the positive direction. The voltage across L_f is $-(n_1 DV_{IN} + V_{C1})$, so i_{D1} is given by

$$\begin{aligned} i_{D1}(t) &= i_{D1}(t_4) - \frac{n_1 DV_{IN} + V_{C1}}{L_f}(t - t_4) \\ &= \frac{n_1(1-D)V_{IN} - v_{C1}(t_1)}{\sqrt{L_f/(C_1 + C_2)}} \cdot \sin\left[\omega_r(t_4 - t_1)\right] \\ &\quad - \frac{n_1 DV_{IN} + V_{C1}}{L_f}(t - t_4). \end{aligned} \tag{3}$$

The current i_{S2} flowing through S_2 is a sum of i_m and i_{pri}, so i_{S2} is given by

$$i_{S2}(t) = -i_m(t) - i_{pri}(t) = -i_m(t) - n_1 \cdot i_{D1}(t).$$

This mode ends when i_{D1} = 0 A, and its duration is short

because the energy stored in L_f is small.

Mode 6 [Fig. 3(f), $t_5 < t < t_6$]: At $t = t_5$, D_1 turns off, D_2 turns on, and D_{S2} remains on. S_2 turns on subsequently at some $t > t_5$. i_{D2} starts to flow as L_f resonates with C_1 and C_2, so

$$i_{D2}(t) = \frac{n_2 DV_{IN} - v_{C2}(t_5)}{\sqrt{L_f/(C_1 + C_2)}} \cdot \sin\left[\omega_r (t - t_5)\right] \tag{4}$$

and

$$i_{S2}(t) = -i_m(t) - i_{pri}(t) = -i_m(t) + n_2 \cdot i_{D2}(t)$$

for $t_5 < t < t_7$.

Mode 7 [Fig. 3(g), $t_6 < t < t_7$]: S_2 has been turned on at $t < t_6$. D_{S2} is turned off when $i_m = -i_{pri}$ at $t = t_6$. The energy stored in L_m is transferred to the output and i_m decreases. Then, the energy stored in L_f is transferred to the output when $i_m < 0$ A. i_{D2} is the same as (4). This mode ends when S_2 is turned off.

The difference of input voltages of transformer causes $V_{C1} \neq V_{C2}$, if $n_1 = n_2$. So, the proposed converter was designed to have $n_1 < n_2$, to operate in the state of $V_{C1} \approx V_{C2} \approx V_O/2$. Using the condition that the average voltages of $v_{Lf}(t)$ should be 0 V both for the $(D+\alpha)T_S$ period at which D_1 turns on, and for the $(1\text{-}D\text{-}\alpha)T_S$ period at which D_2 turns on, the turn ratios n_1 and n_2 of transformer are obtained as

$$n_1 = \frac{V_O(D+\alpha)}{2DV_{IN}(1-D-\alpha)} \tag{5}$$

and

$$n_2 = \frac{V_O}{2DV_{IN}}. \tag{6}$$

($v_{Lf}(t) = n_1(1-D)V_{IN} - V_O/2$ for $t_0 < t < t_4$, $-n_1 DV_{IN} - V_O/2$ for $t_4 < t < t_5$, and $-n_2 DV_{IN} + V_O/2$ for $t_5 < t < T_S + t_1$).

α is determined using (2) and (3) as

$$\alpha = \frac{n_1(1-D)V_{IN} - V_O/2 + T_S I_O/4C_r}{T_S(n_1 DV_{IN} + V_O/2)} \times \sqrt{2L_f C_r} \cdot \sin(\omega_r DT_S) \tag{7}$$

where $C_r = C_1 = C_2$. Then voltage conversion ratio is calculated using the volt-second balance law of L_f for one switching period T_S as

$$\frac{V_O}{V_{IN}} = (n_2 - n_1)\frac{D(1-D-\alpha)}{0.5 - D - \alpha}.$$

The output current I_O is calculated by using (4) and (6) as

$$I_O = \frac{1}{T_S}\int_{t_1}^{T_S+t_1} i_{D2}(t)dt = \frac{1}{T_S}\int_{t_5}^{T_S+t_1} i_{D2}(t)dt = \frac{V_O/2 - v_{C2}(t_5)}{T_S} 2(C_1 + C_2),$$

which results in

$$v_{C2}(t_5) = \frac{V_O}{2} - \frac{T_S I_O}{2(C_1 + C_2)} = v_{C1}(t_1)$$

because $v_{C1}(t) = V_O - v_{C2}(t)$.

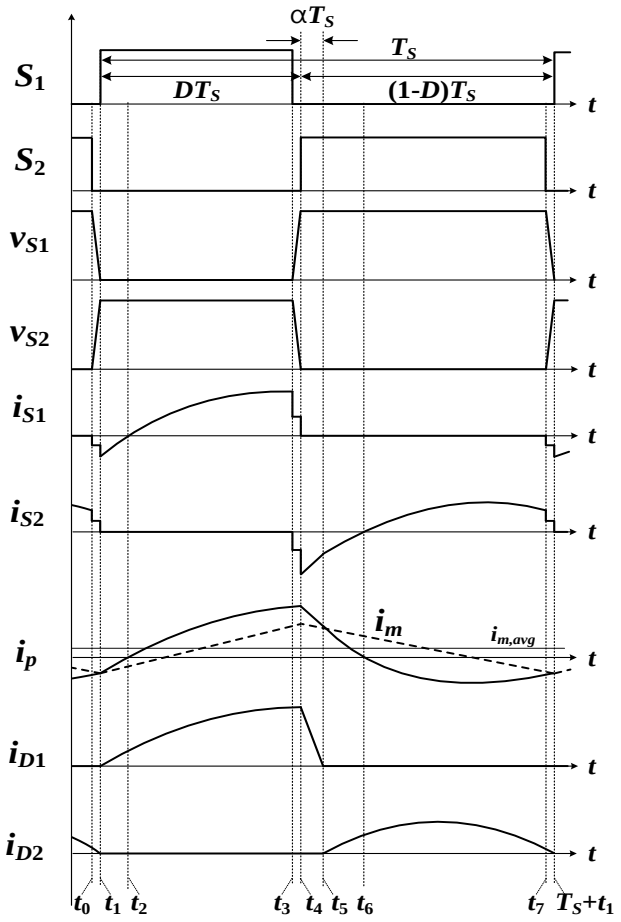


Fig. 4. Operational waveforms of the proposed converter.

III. Design Considerations

A. Forward Inductor L_f

The average value of $i_{D2}(t) = I_O$, so the following equation is obtained using (4):

$$I_O = < i_{D2} > = \frac{1}{T_S}\int_{t_5}^{T_S+t_1} \frac{n_2 DV_{IN} - v_{C2}(t_5)}{\sqrt{L_f/2C_r}} \cdot \sin\left[\omega_r (t - t_5)\right] dt.$$

The converter should handle the maximum output current $I_{O,max}$, so $I_O \le I_{O,max}$. Also, the condition $\pi \le \omega_r(1-D-\alpha)T_S$ must be satisfied to achieve ZCS of D_2. These two conditions result in the following design guide for L_f:

$$\left[\frac{2(1-D-\alpha)\left[n_2 DV_{IN} - V_O/2 + T_S I_{O,\max}/4C_r\right]}{\pi I_{O,\max}}\right]^2 (2C_r) \le L_f < \frac{(1-D-\alpha)^2 T_S^2}{2\pi^2 C_r} \tag{8}$$

B. Resonant Capacitors C_1 and C_2

If $C_1 = C_2 = C_r$, the ripple voltage of C_1 and C_2 is

$$\Delta V_{C1} = \Delta V_{C2} = \frac{1}{2C_r}\int_{t_5}^{T_S+t_1} i_{D2}(t)dt.$$

This equation yields

TABLE I
VALUES OF COMPONENTS FOR THE EXPERIMENTAL CONVERTERS

Components		Proposed converter	Flyback converter	Conventional AHB Converter	Converter of [20]	Converter of [24]
Transformer core		EER 4042	EER 4042	EER 4042	EER 4042	EER 4042
Turn ratios ($1 : n_1 : n_2$)		1 : 0.31 : 0.59	1 : 0.42	1 : 0.8 : 0.8	1 : 0.45	1 : 0.26
Magnetizing inductance (L_m)		793 μH	1.1 mH	451 μH	383 μH	480 μH
Output inductor (L_O)				124 μH		
Leakage inductor	(L_{lk1})			26 μH	64 μH	
	(L_{lk2})					1 μH
Forward inductor (L_f)		9.7 μH				
Blocking capacitor (C_B)		220 nF		220 nF	220 nF	
Clamp capacitor (C_C)						1 μF
Resonant capacitors (C_1, C_2)		220 nF			1 μF	220 nF
Output capacitor (C_O)		220 μF	220 μF	220 μF	220 μF	220 μF
Primary switches	(S_1)	FCPF11N60	STP6N120K3	FCPF11N60	FCPF11N60	FCPF11N60
	(S_2)	FCPF11N60		FCPF11N60	FCPF11N60	FCPF11N60
Rectifier diodes	(D_1)	15ETH06	15ETH06	MUR8100	15ETH06	15ETH06
	(D_2)	15ETH06		MUR8100	15ETH06	15ETH06

$$C_r \geq \frac{T_S I_{O,\max}}{2\Delta V_{C2}} \quad (9)$$

when the ripple voltage ΔV_{C2} is allowed for a stable operation of the circuit; ΔV_{C2} should be less than 30% of $V_O/2$, which is an average of v_{C2}. (When $C_1 = C_2 = 200$ nF and $C_O = 200$ μF, $\Delta V_{C2} = 0.15V_O$ produces an output voltage ripple $\Delta V_O = \Delta V_{C2}C_1/(C_O + C_1) \approx 10^{-3}\Delta V_{C2} = 21.3$ mV at $V_O = 142$ V, which should be acceptable for many applications.)

C. Magnetizing Inductance L_m

$i_{pri}(t_1) = 0$ A and $i_m(t_1)$ should be negative to charge C_{S2}. Also, $i_{S1}(t_1) < 0$ A is required to achieve ZVS turn-on of S_1. Using (1) and the fact that the average value of i_m is $(n_2 - n_1)I_O$ yields

$$i_{S1}(t_1) = (n_2 - n_1)I_O - \frac{(1-D)V_{IN}}{2L_m}DT_S < 0.$$

This condition results in

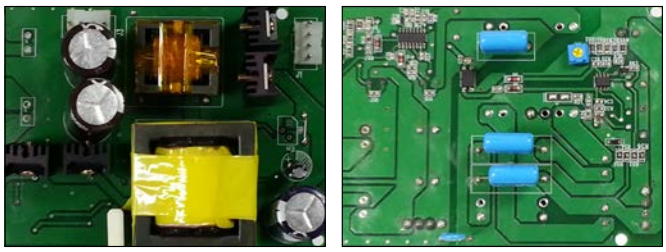
$$L_m < \frac{(1-D)V_{IN}DT_S}{2(n_2 - n_1)I_O}. \quad (10)$$

When this condition is satisfied, S_2 turns on at ZVS condition because $i_{D1}(t_4) > 0$ A and $i_{S2}(t_4) < 0$ A.

IV. EXPERIMENTAL RESULTS

The proposed circuit (Fig. 5) was designed to operate at $V_{IN} =$ 330 ~ 440 V, $V_O = 142$ V, $10 \leq P_O \leq 100$ W, $f_S = 100$ kHz and $0.12 \leq D \leq 0.5$. To determine circuit parameters, D was assumed to be 0.31 at $V_{IN} = 385$ V which is the median value of V_{IN}. $n_2 = 0.59$ was determined using (6) and $C_r = 220$ nF was determined using (9) and $I_{O,max} = 0.7$ A. The value of α in (7) should be a positive number, so

$$n_1 > \frac{V_O/2 - T_S I_{O,\max}/4C_r}{(1-D)V_{IN}} = 0.3.$$



(a) **(b)**

Fig. 5. Photograph of the proposed converter: (a) top and (b) bottom sides.

Based on this constraint, n_1 was chosen as 0.31. Then $L_f = 9.7$ μH and $L_m = 793$ μH were chosen using (8) and (10), respectively. The determined circuit parameters resulted in $\alpha \approx 0.03$ when calculated using (7), then $n_1 \approx 0.31$ was proved by using (5).

The flyback and AHB converters, and the converters of [20] and [24] were built and tested to compare these converters with the proposed one. The components and circuit parameters for all converters are given in Table I. The circuit parameters were optimized to operate at $V_{IN} = 390$ V, $V_O = 142$ V, $f_S = 100$ kHz, and $P_O = 100$ W, following the design considerations in [2], [16], [20], and [24]. For the flyback converter [2], the turn ratio was determined as 1 : 0.42 after considering $V_O/V_{IN} = nD/(1 - D)$ and D should be ~0.5 because the converter operates at a fixed-duty variable-frequency control mode. L_m was determined as 1.1 mH to operate in critical conduction mode (CRM), and the switch STP6N120K3 was chosen to endure the voltage stress. For the conventional AHB converter [16], the turn ratios were determined as 1 : 0.8 : 0.8 after considering $V_O/V_{IN} = D(1 - D)(n_1 + n_2)$ and $D = 0.36$ because the converter has a duty loss problem. L_m, L_{lk1}, and L_O were determined as 451, 26, and 124 μH, respectively, and the diode MUR8100 was adapted to endure the voltage stress. For the converter of [20], the turn ratio was determined as 1 : 0.45 after using V_O/V_{IN}

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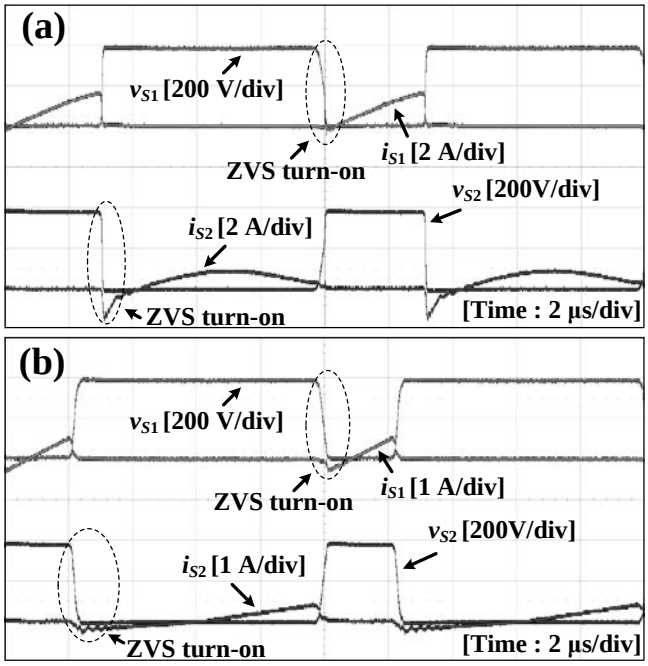

Fig. 6. Voltage and current waveforms of switches of the proposed converter at (a) P_O = 100 W and (b) P_O = 10 W.

≈ $4nD(1 - D)$ and D = 0.31, which is the same D for the proposed converter, to have a fair comparison. L_{lk1} was determined as 64 μH to have I_O = 0.7 A at P_O = 100 W. L_m = 383 μH was chosen to achieve ZVS of switches. For the converter of [24], the turn ratio was determined as 1 : 0.26 after using V_O/V_{IN} ≈ $n/(1 - D)$ and D = 0.31. L_m = 480 μH was chosen to achieve ZVS of switches, and L_{lk2} = 1 μH and C_1 = C_2 = 200 nF were chosen after considering the resonance condition between L_{lk2} and C_1, and C_2 at f_S = 100 kHz.

The voltage and current waveforms of switches in the proposed converter were measured at V_{IN} = 390 V and P_O = 100 W (Fig. 6(a)), and at V_{IN} = 390 V and P_O = 10 W (Fig. 6(b)). The switches subjected to voltage stress of 390 V had ZVS turn-on at P_O = 10 and 100 W.

The voltage and current waveforms of D_1 and D_2 for the proposed converter (Fig. 7(a)), the conventional AHB converter (Fig. 7(b)), and the converter of [20] (Fig. 7(c)) were measured at P_O = 100 W. The proposed converter had much less voltage ringing than the AHB converter, and did not have the duty loss period, which the AHB converter has; η_e decreases when a converter has a duty loss period during which the rectifier diodes are freewheeling. The voltage stress of D_2 of the proposed converter was measured as 240 V, whereas that of the AHB converter was 830 V. Comparing with the converter of [20], the proposed converter had ZCS turn-off for D_2 by using resonance with L_f, C_1, and C_2. But, the converter of [20] could not prevent the hard-switching of D_2 due to energy relaxation time for L_{lk1}, which decreases η_e. The voltage stress of D_2 of the proposed converter was ~50% higher than that of the converter of [20] because $n_1 < n_2$ for the proposed converter.

The η_e versus P_O curves (Fig. 8) were measured for the following converters: flyback, AHB, AHB with voltage doubler (the converter of [20]), dual resonant (the converter of [24]), and proposed converters. The proposed, AHB, and

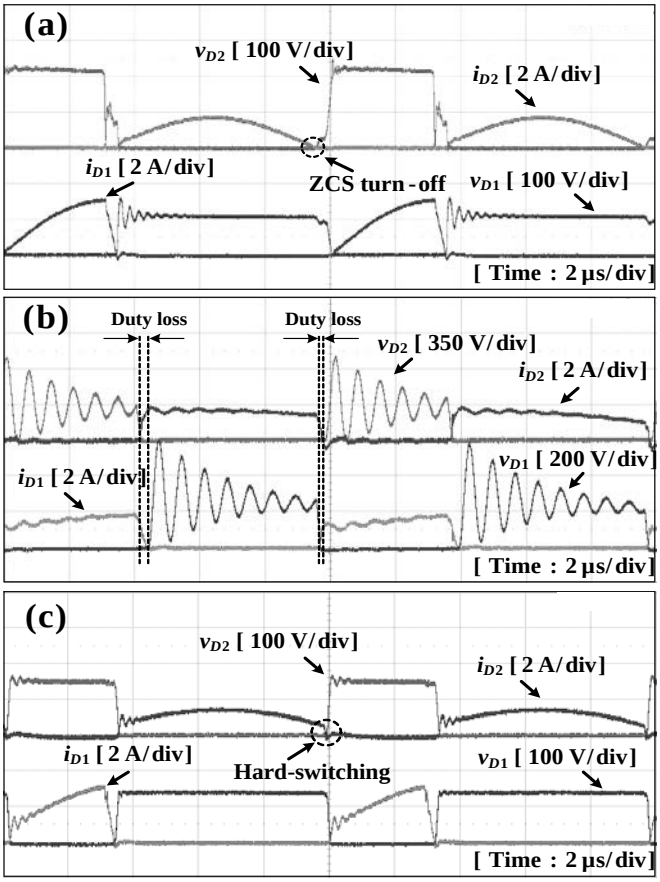

Fig. 7. Voltage and current waveforms of D_1 and D_2 at P_O = 100 W: (a) the proposed converter, (b) the conventional AHB converter, and (c) the converter of [20].

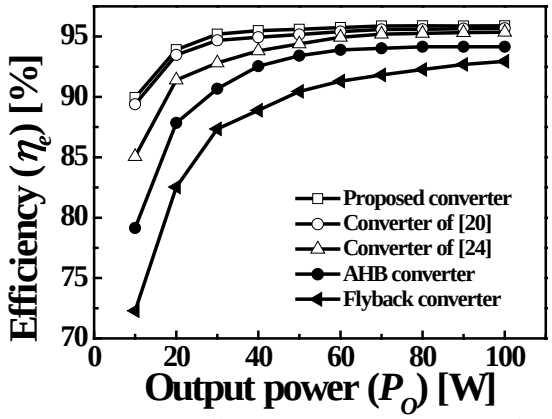

Fig. 8. Power-conversion efficiency η_e versus output power P_O for the flyback converter, the AHB converter, the converters of [20] and [24], and the proposed converter, measured at V_{IN} = 390 V, V_O = 142 V, and P_O = 10 ~ 100 W.

flyback converters had η_e = 95.9, 94.2, and 93.1% at P_O = 100 W, respectively, and had η_e = 90, 79, and 72% at P_O = 10 W. The converters of [20] and [24] had η_e = 95.7 and 95.4% at P_O = 100 W, respectively, and had η_e = 89 and 85% at P_O = 10 W. η_e of the flyback converter decreased rapidly as P_O decreased, because f_S increased at a low P_O. The proposed converter had the highest η_e because it has no duty loss period and its switches and diodes are soft-switched. The converter of [24] had lower

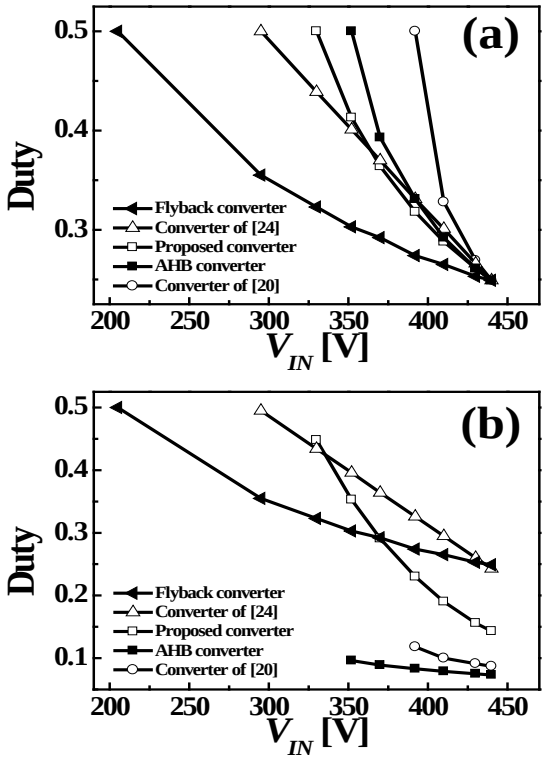

Fig. 9. Duty ratio versus input voltage (a) at P_O = 100 W and (b) at P_O = 10 W.

η_e than the proposed converter because the diodes in the former were subjected to a high current stress, although all switches and diodes were soft-switched. The converter of [20] had η_e very close to that of the proposed converter because L_f of the proposed converter was placed on the secondary stage where the current level was high, and it had no dc-offset current of L_m.

D for V_O = 142 V was measured at P_O = 100 W (Fig. 9(a)) and P_O = 10 W, while varying V_{IN} (Fig. 9(b)). The flyback converter had the widest range of V_{IN} ($205 \le V_{IN} \le 440$ V) because it changed f_S. The input voltage range of the converter of [24] was quite wide ($295 \le V_{IN} \le 440$ V) because the converter has an active clamp structure in the primary stage which clamps the transformer input voltage at $+V_{IN}$ and $-DV_{IN}/(1-D)$. The active clamper reduced also the variation of the duty ratio with P_O. The converters that use the AHB structure in the primary stage had an input voltage range of $352 \le V_{IN} \le 440$ V for the AHB converter and $392 \le V_{IN} \le 440$ V for converter of [20] because they had a duty loss period which is a time interval to discharge the energy stored in L_{lk1}. The duty loss period of the converter of [20] was longer than that of the AHB converter, so the AHB converter had wider input voltage range; the AHB converter requires smaller L_{lk1} than does the converter of [20]. The proposed converter does not require any duty loss period so it had wider input voltage range of $330 \le V_{IN} \le 440$ V than the AHB converter. From this results, the hold-up time $t_{hold} \approx C_{IN}(V_{nom}^2 - V_{\min}^2)/(2P_O)$ for V_O = 142 V, P_O = 100 W, and C_{IN} = 100 μF was calculated as 42 ms for proposed converter and 20 ms for converter of [20].

At V_{IN} = 390 V, V_O = 142 V, P_O = 100 W, f_S = 100 kHz, and D = 0.31, the calculated and measured electrical properties of the proposed converter were compared with those of the converter of [20] and [24] (Table II). (The measured values are given in parenthesis.) When compared with the converters of [20] and [24], the proposed converter had lower voltage stresses on S_1 and S_2, but higher voltage stress on D_2; the converter of [24] was subjected to the highest voltage stresses on S_1 and S_2 because of the active clamp structure in the primary stage, and the proposed converter had different voltage stresses for D_1 and D_2 because of unbalanced secondary turns of transformer. The converter of [20] had higher current stresses on S_1 and S_2 than did the other converters because it did not use a resonance in the secondary stage. D_2 of the converter of [24] had much higher current stress than those of the others because it operated in a discontinuous conduction mode, so the converter of [24] had lower η_e than the others.

TABLE II
VOLTAGE AND CURRENT STRESSES OF SWITCHES AND DIODES IN THE DC-DC CONVERTERS USING VOLTAGE DOUBLER STRUCTURE

		Proposed converter	Converter of [20]	Converter of [24]
Number of components		9	9	9
Voltage stress [V]	S_1, S_2	390 (390)	390 (390)	557 (580)
	D_1	112 (150)	142 (142)	142 (150)
	D_2	224 (240)	142 (160)	142 (154)
Current stress [A]	S_1	1.81 (1.61)	2.15 (2.27)	1.19 (1.62)
	S_2	0.89 (0.90)	1.11 (1.42)	0.57 (0.83)
	D_1	3.25 (3.11)	3.92 (3.20)	3.62 (4.12)
	D_2	1.72 (1.79)	1.39 (1.52)	3.64 (4.10)

V. CONCLUSION

The proposed asymmetric forward-flyback dc-dc converter had high power conversion efficiency η_e for a wide range of output power P_O. The problems of voltage ringing and duty loss in the conventional AHB converter was solved by adopting a forward inductor L_f in the voltage doubler circuit of the secondary stage. The proposed converter used an unbalanced secondary turns of transformer which allowed it to operate for a much wider range of input voltage than the other converter [20] that uses a voltage doubler structure in the secondary stage. The proposed converter also reduced the voltage stress on switches and the current stress on diodes significantly compared to the dual resonant converter (the converter of [24]). The proposed converter had $\eta_e \ge 90\%$ for $10 \le P_O \le 100$ W at V_{IN} = 390 V, V_O = 142 V, and f_S = 100 kHz (the highest η_e = 95.9%, at P_O = 100 W), and could operate at $330 \le V_{IN} \le 440$ V. The proposed asymmetric forward-flyback dc-dc converter is a good candidate for developing a step-down dc-dc converter for applications that require high power-conversion efficiency over wide ranges of input voltage and output power.

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