This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2016.2626383, IEEE Transactions on Power Electronics

Ultra-Large Gain Step-Up Coupled Inductor DC-DC Converter With Asymmetric Voltage Multiplier Network for a Sustainable Energy System

Jian Ai, Mingyao Lin, *Member, IEEE*
(jianai0204@126.com, mylin@seu.edu.cn)
(School of Electrical Engineering, Southeast University, Nanjing 210096, China)

***Abstract*—In this letter, a novel ultra-large gain step-up coupled inductor DC/DC converter with asymmetric voltage multiplier network is presented for a sustainable energy system. The proposed converter contains one boost converter, one voltage multiplier network and one passive lossless clamped circuit. In order to achieve a ultra-large voltage gain, one of the two capacitors is charged by the primary side and secondary side of coupled inductor, then it together with the secondary side of coupled inductor provide its energy for the other capacitor in voltage multiplier network. Besides, the passive lossless clamped circuit not only recycles leakage energy but also effectively reduces the voltage stress on the main switch. By this way, the efficiency of the conversion can be improved. Moreover, the reverse-recovery problem of the diodes in the leakage inductor is alleviated. The operating principles and steady-state analyses are illustrated in detail. Then, the performance of proposed converter is compared with existing converters. Finally, a prototype circuit at 50 kHz switching frequency with 20-V input voltage, 200-V output voltage, $N = 2$, and 200-W output power is established in the laboratory to verify the performance of the proposed converter.**

Index Terms— High step-up voltage gain, asymmetric voltage multiplier network, coupled inductor, DC-DC converter.

I.INTRODUCTION

As the energy crisis and environment pollution becomes more and more serious, renewable energy becomes increasingly important and prevalent in worldwide, particularly in the distributed generation systems that based on the renewable energy sources, including fuel cells, photovoltaic (PV) panels etc [1]–[3]. Unfortunately, the renewable energy sources cannot provide enough dc voltage for generating ac line voltage. Therefore, the step-up converters have been frequently adopted for these low-power conversion applications.

Theoretically, the high voltage gain can be provided by the boost converter, which adopts an extremely high duty cycle. However, the voltage conversion ratio is restricted by parasitic parameters. At the same time, the extremely high duty cycle in boost converter can cause some questions such as low efficiency, serious diode reverse-recovery problems and EMI.

A great deal of research work has been done to provide a high step-up without a high duty ratio. The high step-up voltage gain can be achieved by a switched capacitor technique [4]–[6]. However, switched capacitor technique can cause a high surge current. Switched inductor technology also extends the voltage gain and reduces the voltage stress of the switch. However, the voltage stress of the switches of converters is still high, and so the high-voltage rated switch induces serious conduction losses [7]. By the voltage lift technique, the high step-up voltage gain can be achieved by the transferred energy from the intermediate capacitor, unfortunately, the voltage and current stresses on the intermediate capacitor are serious[8]-[10]. By the coupled inductor technique, the converters can achieve the high step-up voltage gain by adjusting the turns ratio of coupled inductor [11]-[13]. However, the leakage inductance of the coupled-inductor will cause a high voltage spike on active switches when the switch is turned off. The active clamp circuit is proposed to absorb the energy of voltage spike on active switch, so the voltage spike is effectively reduced, but reduction is efficient and extra cost adds [14]-[16]. Adopting the negative clamp circuit technology [17]-[19] in the converters not only recycle the energy of the leakage inductor to increase efficiency, but also enlarge the voltage gain.

In this paper, a novel high step-up converter, which successfully integrates coupled inductor technology and voltage lift technology, is proposed. The proposed converter can achieve a high step-up voltage gain and reduce the voltage stress of main switch. However, the leakage inductor of the coupled inductor may cause high power loss and voltage spike. Thus, a passive lossless clamped circuit that is the part of the proposed is introduced, and it not only can recycle leakage energy and reduce the voltage spike on the main switch, but also improve the voltage gain effectively. Moreover, three diodes have no reverse-recovery problem due to ZCS turn-off, the reverse-recovery problem of the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2016.2626383, IEEE Transactions on Power Electronics

output diode is also alleviated by the leakage inductor. Thus, the performance of the proposed converter can be further improved.

II. BASIC OPERATING PRINCIPLE

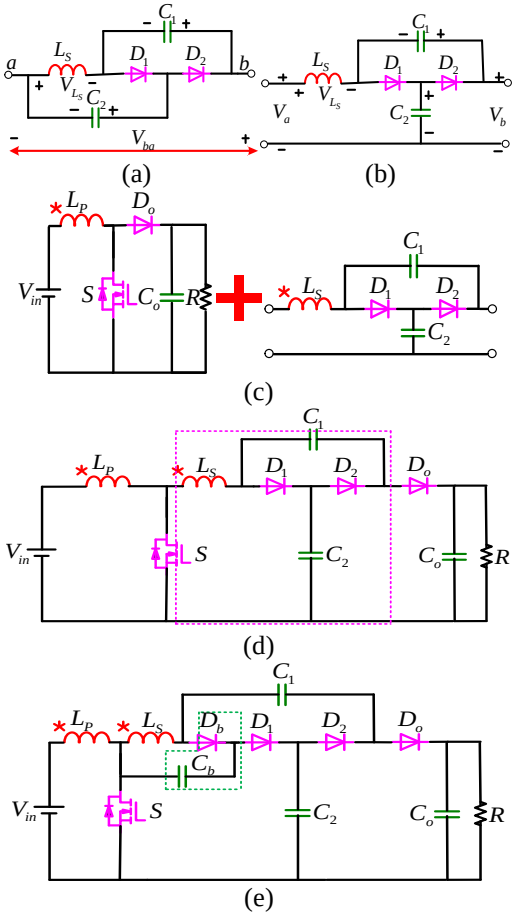

Fig.1 Proposed converter formation process.

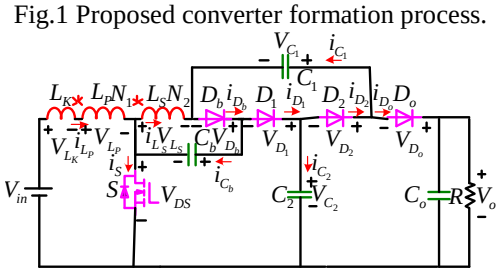

Fig.2 Equivalent circuits of the proposed converter

Fig. 1(a) shows the asymmetric voltage multiplier cell (AVM-cell). The AVM-cell contains one VL-cell, one capacitor and one diode. The voltage of two capacitors is not equal and the two diodes are not turned on at the same time. The asymmetric voltage multiplier network (AVMN) can be obtained though breaking connection point between C_2 and L_S .The VMN is shown in Fig. 1(b).

By combining the asymmetric voltage multiplier network (AVMN) with the traditional boost converter in Fig. 1(c), the converter with the AVMN is proposed as shown in Fig. 1(d). However, the problems can be caused by the leakage inductor, such as high voltage spikes, low efficiency and EMI. In order to recycle the energy of the leakage inductor, restrain voltage spikes and upgrade the efficiency, the passive lossless clamped circuit is introduced as shown in Fig. 1(e).

The equivalent circuit of the proposed converter is shown in Fig.2. To simplify the circuit analysis of the proposed converter, the following conditions are assumed:

1) Capacitors C_1 , C_2 and C_o are large enough so that the voltages on them are considered to be constant in one switching period.

2) The voltage drops across switch and diodes are all zero, and the parasitic of the switch is neglected.

3) The coupling coefficient K of the coupled inductor with turns ratio N. is equals to $L_M \big/ \left(L_M + L_{K_1}\right)$.

During one switching period, the key typical waveforms are briefly illustrated in continuous-conduction-mode (*CCM*) operation, as shown in Fig.3. The operating principle is described as follows:

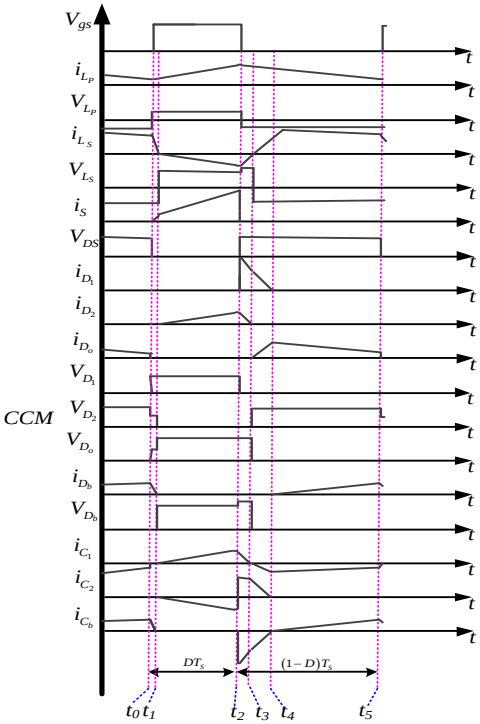

Fig.3 Some typical waveforms of the proposed converter at CCM operation.

1) Mode I [t_0 , t_1]: As shown in Fig. 4(a), the switch S is turned ON. The diode D_b is turned ON, D_1 , D_2 and D_o are turned OFF. The current i_{L_p} is still increased, the clamp capacitor C_b is still charged by secondary-side winding. Moreover, the output capacitor C_o provides its energy to the load. When the current of the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2016.2626383, IEEE Transactions on Power Electronics

secondary-side winding is equal to zero, this operation ends.

2) Mode II [t_1, t_2]: During this time interval, the switch S is still turned ON. The diode D_2 is turned ON, the diodes D_1, D_b and D_o are turned OFF. The current-flow path is shown in Fig. 4(b). The capacitor C_1 is charged by secondary-side winding L_S and capacitor C_2. Besides, the energy needed by the load is supplied by the output capacitor C_o. When switch S is turned OFF, this operating mode ends. Therefore, V_{C_1} can be expressed to be

$$V_{C_1} = NV_{L_P}^{\mathrm{II}} + V_{C_2} \tag{1}$$

3) Mode III [t_2, t_3]: At $t = t_2$, D_1 and D_2 are turned ON, moreover, D_b and D_o are turned OFF. The current-flow path is shown in Fig. 4(c). The capacitor C_2 is charged by input source, primary winding and clamp capacitor C_b. Therefore, the passive lossless clamped circuit not only recycles leakage energy but also effectively reduces the voltage spike on the switch S. Besides, the capacitor C_1 is charged by secondary-side winding L_S and the capacitor C_b though diodes D_1 and D_2. As soon as the current i_{D_2} is equal to zero, the operation goes to mode IV.

4) Mode IV [t_3, t_4]: During this time interval, the switch S is still turned OFF. Diodes D_b and D_2 are still turned OFF. Besides, the diodes D_1 and D_o are turned ON. The current-flow path is shown in Fig. 4(d). Therefore, the energy that is from the input source, the secondary-side winding and the primary-side winding of the coupled inductor and C_1 is released to the output capacitor C_o and load. At the same time, the capacitor C_2 is charged by the input source and clamp capacitor C_b. When current i_{D_1} is equal to zero, this mode ends. Therefore, V_{C_b} and V_o can be expressed as

$$V_{C_2} = V_{in} - V_{L_K}^{\mathrm{IV}} - V_{L_P}^{\mathrm{IV}} + V_{C_b} \tag{2}$$

$$V_o = V_{in} - V_{L_K}^{\mathrm{IV}} - (N+1)V_{L_P}^{\mathrm{IV}} + V_{C_1} \tag{3}$$

5) Mode V [t_4, t_5]: At $t = t_4$, During this time interval, the switch S is still turned OFF, and diodes D_1 and D_2 are turned OFF. The current-flow path is shown in Fig. 4(e).Besides, the clamp diode D_b and output diode D_o is turned ON. Therefore, the secondary-side winding L_S charge the clamp capacitor C_b via clamp diode D_b. Also, the input source, primary-side winding, secondary-side winding and C_1 provide their energy to C_o and load, the current of the primary-side winding decreases. Therefore, V_{C_b} and $V_{L_P}^{\mathrm{V}}$ can be expressed as

$$V_{C_b} = -NV_{L_P}^{\mathrm{V}} \tag{4}$$

$$V_{L_P}^{\mathrm{IV}} = V_{L_P}^{\mathrm{V}} \tag{5}$$

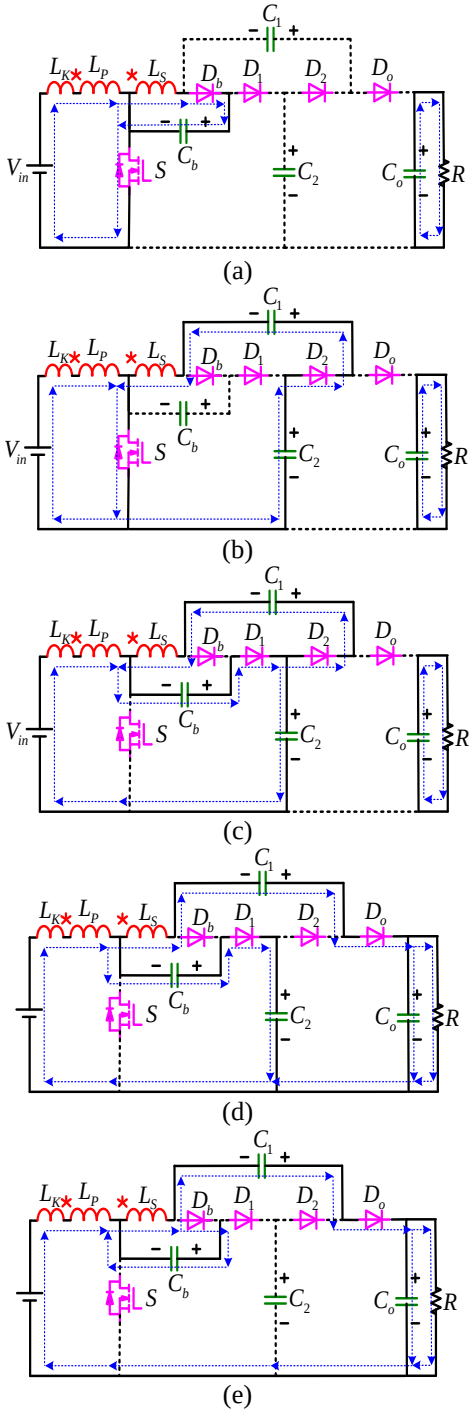

Fig.4 Current-flow path of the operating modes during one switching period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2016.2626383, IEEE Transactions on Power Electronics

III.CIRCUIT PERFORMANCE ANALYSIS

A. Steady-State Analysis

To simplify the calculation, the time durations of modes I and III are very short when compared to one switching period at CCM operation. Thus, only modes II, IV, and V are considered.

During mode II, the following equations that based on Fig. 4(b) can be written:

$$V_{L_P}^{\mathrm{II}} = KV_{in} \tag{6}$$

$$V_{L_K}^{\mathrm{II}} = (1-K)V_{in} \tag{7}$$

Using the volt–second balance principle on L_P and L_K to yield

$$\int_{t_1}^{t_2} V_{L_P}^{\mathrm{II}}\,dt + \int_{t_3}^{t_4} V_{L_P}^{\mathrm{IV}}\,dt + \int_{t_4}^{t_5} V_{L_P}^{\mathrm{V}}\,dt = 0 \tag{8}$$

$$\int_{t_1}^{t_2} V_{L_K}^{\mathrm{II}}\,dt + \int_{t_3}^{t_4} V_{L_K}^{\mathrm{IV}}\,dt + \int_{t_4}^{t_5} V_{L_K}^{\mathrm{V}}\,dt = 0 \tag{9}$$

Substituting (1)-(7) into (8) and (9), the voltage gain can be obtained as

$$M_{CCM} = \frac{2+NK+NDK}{1-D} \tag{10}$$

It can be seen that the voltage gain is influenced by the turns ratio and leakage coefficient. The relationship among the voltage gain, the duty ratio and the coupling coefficients of coupled inductor is shown in Fig.5. If the impact of the leakage inductances of the coupled inductor is neglected, coupled coefficient K is equal to 1. The ideal voltage gain can be obtained as

$$M_{CCM} = \frac{2+N+ND}{1-D} \tag{11}$$

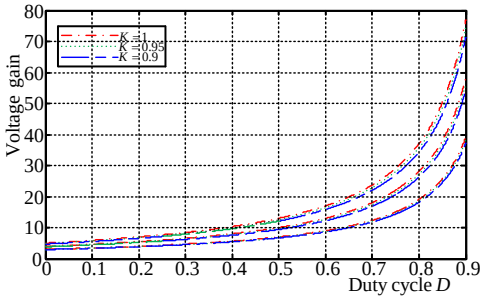

Fig.5 The effect of leakage inductance and turns ratio on voltage.

B. Voltage Stresses and Current Stresses on Power Devices

In the proposed converter, the voltage of the capacitors is a constant and the leakage inductance is ignored to simplify the voltage stresses analysis on the components. The voltage stresses across the switch S and the D_1 and D_2 diodes are derived by

$$V_{DS} = \frac{V_o}{2+N+ND} \tag{12}$$

$$V_{D_1} = \frac{V_o}{2+N+ND} \tag{13}$$

$$V_{D_2} = \frac{(1+N)V_o}{2+N+ND} \tag{14}$$

The capacitors C_1 and C_2 can be expressed as

$$V_{C_1} = \frac{(1+N)V_o}{2+N+ND} \tag{15}$$

$$V_{C_2} = \frac{(1+ND)V_o}{2+N+ND} \tag{16}$$

The voltage of the capacitor C_b and the voltage stresses on diode D_b are given by

$$V_{C_b} = \frac{NDV_o}{2+N+ND} \tag{17}$$

$$V_{D_b} = \frac{NV_o}{2+N+ND} \tag{18}$$

The on-state average current of the output diode D_o is calculated as

$$I_{D_o} = \frac{I_o}{1-D} \tag{19}$$

During one switching period, the electric charge through the capacitors is zero. At mode IV, the duty cycle of the released energy can be approximately obtained

$$D_c = \frac{2(1-D)}{N+2} \tag{20}$$

In order to analyze，the simplified waveforms of the proposed converter are shown in Fig.6. During the time interval $[t_2, t_4]$，the on-state average current of the diode D_1 can be expressed as

$$I_{D_1[t_2-t_4]} = \frac{I_o}{D_c} \tag{21}$$

During the time interval $[t_4, t_5]$，the on-state average current of the diode D_b can be expressed as

$$I_{D_b[t_4-t_5]} = \frac{(N+2)I_o}{N-ND} \tag{22}$$

During the time interval $[t_2, t_5]$，while using KCL, at junction point of the secondary-side L_S of the coupled inductor, diode D_b and capacitor C_1, the currents of secondary-side L_S of the coupled inductor can be written as

$$I_{L_S[t_2-t_5]} = \frac{2(N+1)I_o}{N-ND} \tag{23}$$

During the time interval $[t_0, t_2]$，the currents of secondary-side L_S of the coupled inductor can be obtained

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2016.2626383, IEEE Transactions on Power Electronics

$$I_{L_S[t_0-t_2]}=\frac{I_o}{1-D} \tag{24}$$

During the time interval $[t_2, t_5]$, while using KCL, at junction point of the secondary-side L_P and primary-side L_S of the coupled inductor and capacitor C_b, the currents of primary-side L_P of the coupled inductor can be written as

$$I_{L_P[t_2-t_5]}=\frac{(N+3)I_o}{1-D} \tag{25}$$

According to the magnetic flux conversation principle, the following equations that based on Fig. 6 can be written:

$$I_{L_P[t_0-t_2]}+NI_{L_S[t_0-t_2]}=I_{L_P[t_2-t_5]}+NI_{L_S[t_2-t_5]} \tag{26}$$

Collecting the terms, during the time interval $[t_0, t_2]$, the on-state average currents of primary-side L_P of the coupled inductor can be expressed as

$$I_{L_P[t_0-t_2]}=\frac{(2N+5)I_o}{1-D} \tag{27}$$

So, the RMS value of the switch S is

$$I_{S-RMS}=\frac{(5+2N)\sqrt{D}P_o}{(1-D)V_o}\sqrt{\frac{K_L^2}{12}+1} \tag{28}$$

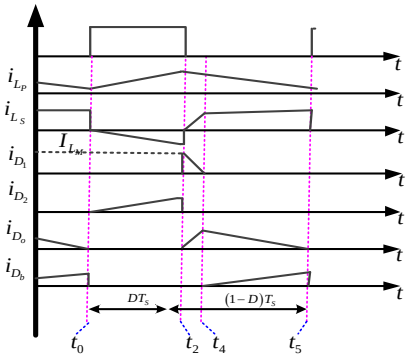

Fig.6 Simplified waveforms

C. Comparison with Other Converters

For demonstrating the performance of the proposed converter, table I shows the performance comparison which the proposed converter is compared with the traditional Boost converter, the converter in [13], the converter in [20] and the converter with AVM-cell as shown in Fig. 7(a)–(c).

When $N=2$, Fig.8 shows the voltage gain against the duty ratio of them, the relationship between the voltage stresses of active switch with variable duty cycle is described in Fig.9, therefore, the relationship between the voltage stresses of output diode with variable duty cycle is described in Fig.10.

Compared the boost converter with the proposed converter with AVMN, the conversion ratios is high. However, the numbers of diodes of the proposed converter with AVMN are more than the boost converter. Fortunately, the voltage stresses of the active switch and output diode of the proposed converter with AVMN are far lower than that of boost converter.

Compared the converter in [13] and the converter with AVM-cell with the proposed converter with AVMN, the quantities of active switch and diode are equal and the output diode voltage stress is higher, but the gain of the converter with AVM-cell is higher than the gain of these converter and the voltage stress of the active switch is lower than voltage stress of active switch of those converter. So, it is beneficial to improve the converter efficiency because low voltage MOSFET with low R_{DS_ON} is available in high step-up and high output voltage application.

When the duty cycle is lower than about 0.4, the conversion ratios of the proposed converter with AVMN is lower than the converter in [20], the numbers of diodes is more, the active switch voltage stress and output diode voltage stress are higher. Fortunately, the numbers of active switch in the proposed converter is lower than that in the converter in [20], the reliability is higher and the cost is lower. When the duty cycle is higher than 0.4, the proposed converter has a higher conversion gain and the active switch voltage and output diode voltage stresses are lower than the converter in [20]. So, low voltage MOSFET with low R_{DS_ON} and low voltage output diode with low R_{ON} are available in high step-up and high output voltage application. It is beneficial to improve the converter efficiency. So, the proposed converter is more suitable for the high step-up and high output voltage application.

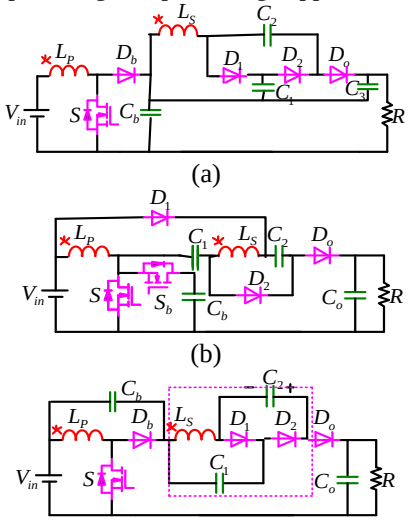

Fig.7 Schematic of the configurations used for comparison purposes: (a) Converter with VL-cell in [13] (b) Converter with VM-cell in [20] (c) Converter with AVM-cell

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2016.2626383, IEEE Transactions on Power Electronics

TABLE I Performance comparison among different converters

Topology	boost	Converter in[13]	Converter in[20]	Converter with AVM-cell	Proposed converter with AVMN
Numbers of active switches	1	1	2	1	1
Numbers of diodes	1	4	3	4	4
Voltage gain	$\frac{1}{1-D}$	$\frac{1+N+ND}{1-D}$	$\frac{(N+1)(2-D)}{1-D}$	$\frac{1+N+ND}{1-D}$	$\frac{2+N+ND}{1-D}$
Voltage stress of active switches	V_o	$\frac{V_o}{1+N+ND}$	$\frac{V_o}{(N+1)(2-D)}$	$\frac{V_o}{1+N+ND}$	$\frac{V_o}{2+N+ND}$
Voltage stress of output diodes	V_o	$\frac{NV_o}{1+N+ND}$	$\frac{(N+1)V_o}{(N+1)(2-D)}$	$\frac{NV_o}{1+N+ND}$	$\frac{(N+1)V_o}{2+N+ND}$

Fig. 8 Voltage gain against duty ratio of the proposed converter, the converter with AVM-cell, the boost converter, the converters in [13] and [20] at CCM operation under K =1 and N =2

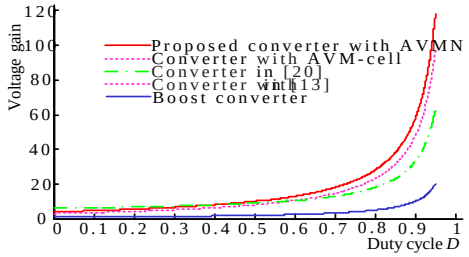

Fig. 8 Voltage gain against duty ratio of the proposed converter, the converter with AVM-cell, the boost converter, the converters in [13] and [20] at CCM operation under K =1 and N =2.

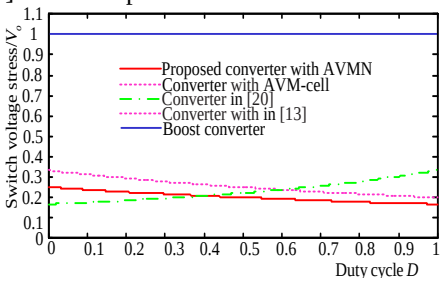

Fig.9 Active switch voltage stress comparison

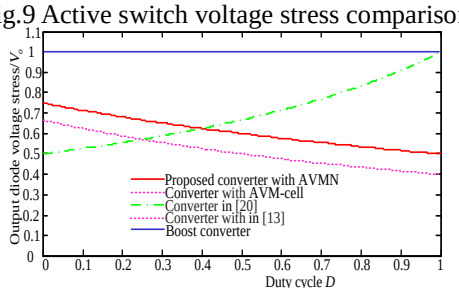

Fig.10 Output diode voltage stress comparison

IV. DESIGN GUIDELINES

A. Turns Ratio Design

Since the turns ratio of the coupled inductor determines the voltage stress of the switch and the operational duty-cycle of the converter, it is the key parameter in the circuit parameter design. A proper turns ratio can be obtained once the duty-cycle is designed (in general, the optimal duty cycle is about 0.4~0.6), which is given by

$$N=\frac{V_o(1-D)-2V_{in}}{V_{in}(1+D)} \tag{29}$$

B. Magnetizing Inductance Design

Thus, based on Fig.6 and equation (20), the magnetic average current of the coupled inductor can be represented by

$$I_{L_M}=\frac{(N+2)I_o}{1-D} \tag{30}$$

The magnetizing inductor can be designed by setting an acceptable current ripple on the magnetizing inductor, which is given by

$$L_M \geq \frac{V_{in}D}{K_{L_M}I_{L_M}f_s} \tag{31}$$

Combining (30) and (31), and collecting the terms, the magnetizing inductance can be computed as

$$L_M \geq \frac{V_{in}D(1-D)}{K_{L_M}(N+2)I_o f_s} \tag{32}$$

Where K_{L_M} is the current ripple coefficient.

C. Output Capacitor Design

The aim of the output capacitor C_o is to limit the output voltage ripple ΔV to a reasonable range. When the switch is turned ON, the capacitor C_o released energy to the load, the electric charge can be written as follows:

$$\Delta Q = I_o DT_s \leq C_o \Delta V \tag{33}$$

Therefore, the output capacitor can be chosen as

$$C_o \geq \frac{V_o D}{\Delta V R f_s} \tag{34}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2016.2626383, IEEE Transactions on Power Electronics

TABLE II System specifications of the proposed converter

System parameters	Specifications
Input voltage V_{in}	20V
Output voltage V_{o}	200V
Rated power P_{o}	200W
Switching frequency f_{s}	50kHz

TABLE III System specifications of the proposed converter

MOSFET Switch S	IRFP4568
Diodes $D_{\text{b}}, D_1, D_2, D_{\text{o}}$	VF30200
Output capacitor C_o	470μF
Capacitors C_1, C_2	2.2μF
Coupling inductors	Core-NPS306060, $N = N_2 : N_1 = 2$, $L_{\text{P}} = 137.6\mu\text{H}, L_{\text{S}} = 548.5\mu\text{H}$

V. EXPERIMENTAL RESULTS

Before this topic is discussed, some specifications are given in TABLE II. Table III shows the component specifications that used in the proposed converter.

Fig. 11 illustrates the measured waveforms when $V_{in} = 20\text{V}$ and $P_o = 200\text{W}$. The voltage stresses of the switch and currents of the primary-side of coupled inductor and secondary-side of coupled inductor are given in Fig. 11(a). The switch duty cycle is about 0.51. According to the measured waveforms, the voltage V_{DS} across the switch is clamped at approximately 40V. This makes the low on-resistance MOSFET available. The current and voltage across diode D_o is shown in Fig. 11(b). It is cleared that the voltage step exists. The current and voltage across diode D_2 is shown in Fig. 11(c). It is cleared that the voltage step exists. The current of diode D_2 decreases to zero before the switch turns off, which means no reverse-recovery problem. The current and voltage across diode D_1 is shown in Fig. 11(d). It is cleared that the voltage step exists. The current of diode D_1 decreases to zero before the switch turns off, which means no reverse-recovery problem. The current and voltage across clamp diode D_b is shown in Fig. 11(e). The current of diode D_b decreases to zero before the switch turns off, which means no reverse-recovery problem.

In order to examine the dynamic response performance of the proposed converter, the experimental results of the output voltage and output current under the step load variation between 50W and 20W are depicted in Fig.12. It can be seen that the output voltage can keep stable to the load condition with a closed loop control. The measured efficiency of the tested 200W prototype with 20V input voltage is shown in Fig. 13. The maximum efficiency is about 97.1% at P_{o}=80 W .

Finally, when $V_{in} = 20\text{V}$, some main experimental and theoretical data are shown in Fig. 14and Fig. 15, respectively.

According to the information in the Fig. 14, the experimental data are very close to the theoretical analysis for main switch voltage stress. Moreover, because the effect of parasitic elements the voltage stress of diode D_1 in experiment is slightly lower than the calculation counterparts in theory.

Meanwhile, compared the theoretical analysis for output diode voltage stress, output diode voltage stress is about three volts less in Figure 15. Therefore, they are very close. So, the experimental results that obtained agree with the theory. According to the information in Fig.15, because the effects of parasitic elements the capacitor C_1 voltage and voltage stress of diode D_2 in experiment are about five volts lower than the calculation counterparts in theory. Besides, compared with the theoretical analysis for capacitor C_1, the voltage stress on capacitor C_1 is about four volts less as shown in Figure 15. They are almost equal. Therefore, the experimental data are corresponding to the theoretical analysis.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2016.2626383, IEEE Transactions on Power Electronics

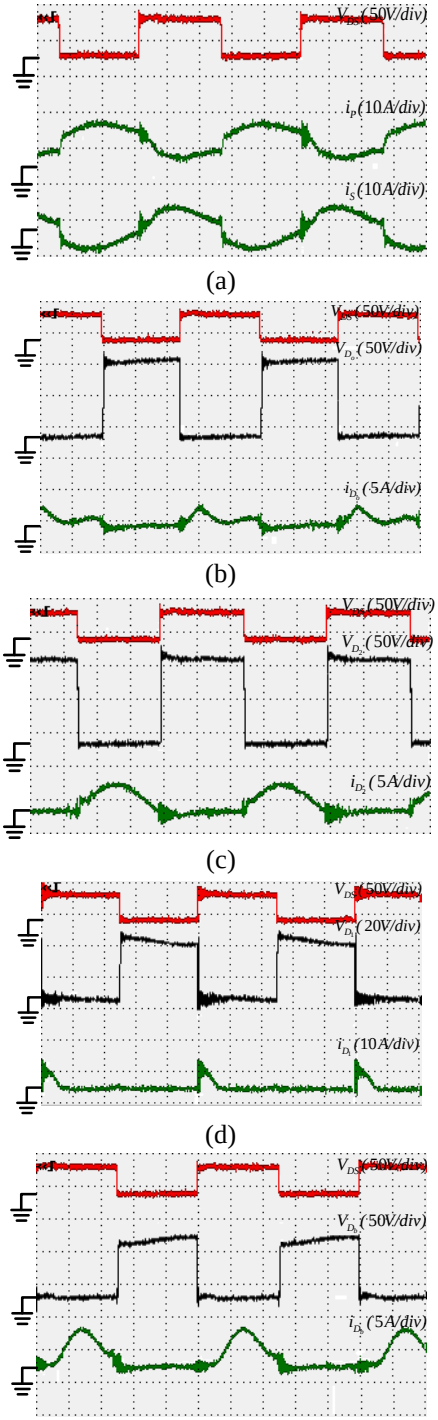

Fig.11 Experiment results under full-load P_o = 200 W.

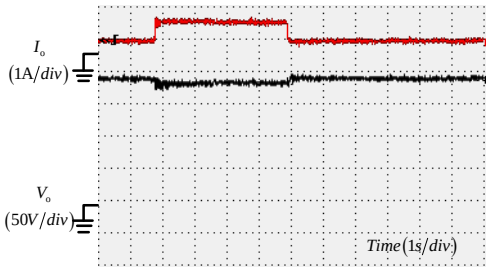

Fig.12 experimental results with step load variation between 50W and 200W

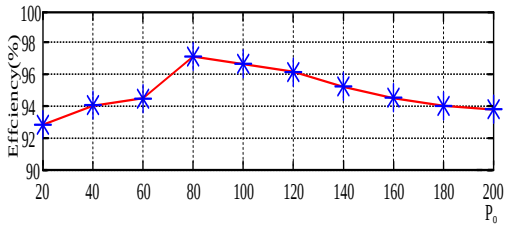

Fig.13 Test efficiency of 200W prototype

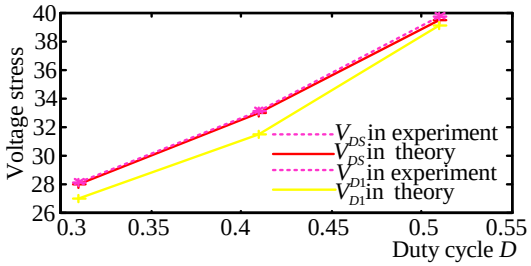

Fig. 14 Voltage stress against duty ratio of the proposed converter

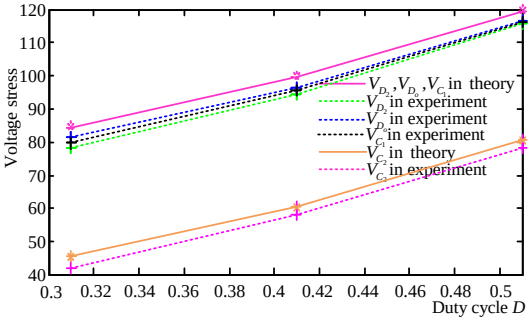

Fig.15 Voltage stress against duty ratio of the proposed converter

VI Conclusion

In this letter, a novel converter is proposed with asymmetric voltage multiplier network. Compared with the Voltage multiplier cell, the VMN is an asymmetric structure. Two diodes turn on in different time zones. Moreover, two capacitors are charged or discharged in different time zones. Besides, the clamped circuit not only reduces the voltage stress on the main switch effectively, but also improves the efficiency. The steady state analysis of the proposed converter with high voltage gain is given. Compared with the traditional high step-up DC-DC converter, it has following main advantages:

1) The proposed converter can achieve a high voltage conversion gain with a relatively small duty cycle, which is helpful to reduce the current stress through the switch and suitable for sustainable energy sources;

2) The diodes D_1, D_2 and D_b achieve turn-off naturally and avoid the reverse-recovery problem;

3) The energy stored in the leakage inductance is recycled to improve the performance of the presented converter.

REFERENCES

[1] J. T. Bialasiewicz, "Renewable energy systems with photovoltaic power generators: Operation and modeling," IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2752–2758, Jul. 2008.

[2] T. Zhou and B. Francois, "Energy Management and power control of a hybrid active wind generator for distributed power generation and grid integration," IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 95–104, Jan. 2011.

[3] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," IEEE Trans. Ind. Electron.,vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[4] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC–DC PWM converters," in IEEE Trans. Circuits Syst. I. vol. 55, no. 2, pp. 687–696, Mar. 2008.

[5] O. Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, "Step-up switching-mode conver -ter with high voltage gain using a switched capacitor circuit," IEEE Trans. Circuits Syst. I, vol. 50, no. 8, pp. 1098–1102, Aug. 2003.

[6] B.Axelrod, Y.Beck and Y.Berkovich:"High step-up DC–DC converter based on the switched-coupled-inductor boost converter and diode-capacitor multiplier: steady state and dynamics," IET Power Electron., vol. 8, pp. 1420–1428, 2015.

[7] Y.Tang, D.J.Fu and T.Wang, "Hybrid Switched-Inductor Converters for High Step-Up Conversion" IEEE Trans. Ind. Electron, vol. 62, no. 3, pp.1480–1490, Mar. 2015.

[8] Y. Jiao, F.L. Luo and M. Zhu, "Voltage-lift-type switched-inductor cells for enhancing DC – DC boost ability: principles and integrations in Luo converter," IET Trans. Power Electron. , vol. 4, no. 1, pp. 131–142, 2001.

[9] B. Axelrod, Y. Berkovich, S. Tapuchi, and A. Ioinovici, "Single-Stage Single-Switch Switched-Capacitor Buck/Buck-Boost-Type Converter", IEEE Trans. Aerospace and Electronic Systems, vol. 45, no. 2, pp.419-430, Apr.2009.

[10]Luo, F.L.: "Six self-lift DC– DC converters, voltage lift technique", IEEE Trans. Ind. Electron., 2001, 48, (6), pp. 1268–1272.

[11]Luo, F.L., Ye, H.: "Positive output super-lift converters", IEEE Trans. Power Electron., 2003, 18, (1), pp. 105–113.

[12]X. Hu, and C. Gong: "A high voltage gain DC-DC converter integrating coupled-inductor and diode-capacitor techniques," IEEE Trans. Power Electron., vol. 29, no. 2, pp. 789–800, Feb. 2014.

[13]B.Axelrod, Y.Beck and Y.Berkovich:"High step-up DC–DC converter based on the switched-coupled-inductor boost converter and diode-capacitor multiplier: steady state and dynamics," IET Power Electron., vol. 8, pp. 1420–1428, 2015.

[14]Y. Berkovich and B. Axelrod: "High step-up DC-DC converter based on the switched-coupled-inductor boost converter and diode-capacitor multiplier," Conf. IET Power Electron., Mar. 2012.

[15]Wu, T.F., Lai, Y.S., Hung, J.C., Chen, Y.M.: "Boost converter with coupled inductors and buck–boost type of active clamp", IEEE Trans. Ind. Electron., 2008, 55, (1), pp.154–162.

[16]Lin, B.R., Hsieh, F.Y.: "Soft-switching zeta–flyback converter with a buck–boost type of active clamp", IEEE Trans. Ind. Electron., 2007,54, (5), pp. 2813–2822.

[17] B. R. Lin and F. Y. Hsieh, "Soft-switching zeta–flyback converter with a buck–boost type of active clamp," IEEE Trans.Ind. Electron., vol. 54, no. 5, pp.2813–2822, Oct.2007.

[18]Y. P. Hsieh, J. F. Chen, T. J. Liang and L. S. Yang: "Novel High Step-Up DC–DC Converter With Coupled-Inductor and Switched-Capacitor Techniques for a Sustainable Energy System", IEEE Trans. Power Electron., vol. 26,no. 12, pp. 3481-3490,Doc. 2011.

[19] Y.P. Hsieh, J.F. Chen, T.J. Liang and L.S. Yang: "Analysis and implementation of a novel single-switch high step-up DC– DC converter", IET Power Electron., Vol. 5, pp.11–21, May 2012.

[20] Hwu.K.I and Yau.Y.T:"High Step-Up Converter Based on Coupling Inductor and Bootstrap Capacitors With Active Clamping," IEEE Trans. Power Electron., 2014, 18, (1), pp. 2655–2660.