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Analysis and Design of Charge Pump Assisted High Step-up Tapped Inductor SEPIC Converter with an "Inductor-less" Regenerative Snubber

***Abstract*— this paper introduces a SEPIC derived converter suited for alternative energy generation applications. The proposed converter utilizes tapped inductor and charge pump techniques to achieve high step up gain and a passive regenerative snubber to attain high efficiency. Compared with earlier counterparts, the proposed converter has the advantage of continuous input current, which can be helpful in attaining accurate tracking of maximum power point of solar panels. The paper presents principle of operation, theoretical analysis, and design guidelines. Theoretical expectations were confirmed by simulation and experimental results.**

***Index Terms*—High step up converter, soft switching, tapped inductor, regenerative snubber.**

I. Introduction

Alternative energy sources such as solar panels and fuel cells generate relatively low dc voltage [1-2]. Grid interconnection of such resources is made possible applying electronic power inverters [3-5]. Traditionally, inverters for alternative energy generation are realized using a two stage power processing scheme, comprised of a high step-up dc–dc front end converter followed by a grid tied dc-ac inverter. Since the grid-tied inverter stage requires rather high dc bus voltage, the dc-dc stage may need to step up the low voltage of the solar panel about tenfold or higher. However, basic dc–dc converters such as boost, buck–boost, Cuk, Sepic, and Zeta cannot provide high efficiency at the required conversion ratio. In a quest for higher voltage gain and efficiency, a number of innovative techniques have been proposed in recent literature. These include application of multipliers [6], switched capacitor/inductor hybrid structures [7], voltage-lift [8] and cascaded boost converters [9]. These methods typically lead to increased component count and cost as well as control complexity.

Tapped inductor (TI) converters are an alternative, which offers simple circuit and low part count. The tapped inductor boost (TI-boost) converter [10], can achieve much higher gain than its basic counterpart just by adjusting the turns ratio. TI can be introduced to other traditional DC-DC converters as well. TI-flyback [11], [12], TI-cascaded boost [13], TI-SEPIC [14], [15], and TI-ZETA [12], [16] topologies have been reported. However, application of the tapped inductor (TI) requires some special consideration. The leakage inductance can cause high-voltage spike across the switch, whereas dissipation of the leakage energy impairs the efficiency. It also impedes secondary current, limits the power transfer to the load and makes the voltage conversion ratio load dependent. To alleviate switch voltage stress and improve converter performance, snubber circuits were employed to properly capture and recycle the leakage energy [17]-[23]. Therefore, a number of approaches were developed to moderate the switch voltage stress and increase the converter's efficiency [24]-[37]. An active snubber was applied to the TI-boost topology by [24]. Modified TI-boost converters using passive snubber to absorb the leakage energy were also shown to achieve comparable efficiency [25], [26]. Other approaches include integration of the tapped inductor and switch capacitor/multiplier cell techniques [26]-[31]; adding extra inductor for continuous input current [30]-[33]; stacking multiple windings [14], [34]; voltage lifting technique incorporated with tapped inductor [35]; while at higher power interleaving technique was adopted [36], [37].

In order to achieve high voltage gain, a tapped inductor boost converter has to be designed with increased turns ratio which

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causes increased pulsation in the input current as well as increased output diode voltage stress and ringing. The pulsed input current penalizes the input source with increased high frequency rms current component that causes higher losses. Furthermore, in photovoltaic (PV) applications, the pulsating input current periodically shifts the operating point and makes it difficult to precisely track the Maximum Power Point (MPP). To minimize the pulsed current problem, an input filter can be used. However, the increased component count of a tapped inductor boost and its LC input filter matches that of a classic SEPIC converter. An interesting feature of the SEPIC converters is that the pulsating current of the tapped inductor circuit does not flows at the input port. Moreover, SEPIC can be designed to operate at continuous input current with relatively low, or even zero, input current ripple [38], a feature that may be of an advantage interfacing PV sources. The low input current ripple keeps the instantaneous operating point in a close vicinity of the true MPP and so helps extracting more power from the PV source. Therefore, although, traditional boost converters can attain higher gain and efficiency than traditional SEPICs, in some applications, the modified SEPIC converters can, possibly, challenge the boost derived converters [39].

The considerations above motivated further investigation of SEPIC derived high step-up converters [40]. A preliminary study of the proposed single switch high efficiency high step-up dc-dc converter topology was undertaken in [41]. In this paper a detailed account is presented. The proposed converter is derived from the basic SEPIC topology by applying a tapped inductor to attain higher voltage gain. Further increase in voltage gain is obtained applying a charge pump. The proposed converter also inherits the SEPIC's advantage of continuous input current. Furthermore, a simple "inductorless" passive regenerative snubber is fitted into the circuit to capture and recycle the leakage energy, suppress the voltage spike and provide lossless switching for the semiconductor switch. Compared with earlier TI-SEPIC topology [15], the proposed converter achieves higher gain by using a charge pump. Furthermore, the incorporated "inductorless" passive regenerative snubber helps the proposed converter attaining zero voltage (ZV) and zero current (ZC) switching, which improve the efficiency, and, potentially, allow higher switching frequency and size reduction. Moreover, the feature of continuous input current and, as a result, lower input voltage ripple across the photovoltaic panel, can be helpful assisting the controller tracking the maximum power point with greater accuracy. These merits make the proposed converter a viable candidate as a front end dc-dc converter for alternative energy generation applications.

This paper is organized as follows. Derivation of the topology is described in section II; steady-state operational analysis is given in Section III, performance analysis and design guidelines are is presented in sections IV and VI respectively. Experimental results of a 200W, 35V-input 380V-output prototype with 60 kHz switching frequency are shown in Section V. Lastly, the comparison with earlier counterpart is conducted in VII.

II. The Proposed Topology

The proposed topology is derived from a traditional single switch SEPIC converter. The proposed converter, shown in Fig. 2, is comprised of an input inductor L_{in}, a buffer capacitor C_1, and a tapped inductor L_1, L_2 . A charge pump is fitted into the circuit, which consists of C_2, D_1 and D_o, feeding an output filter capacitor, C_o, and a load, R_L.

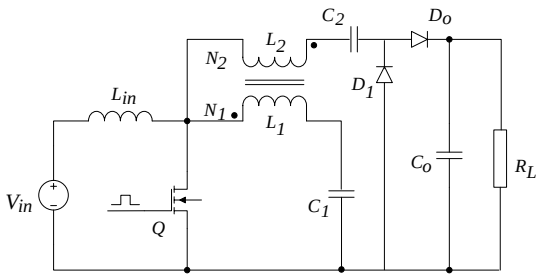

Fig. 1. Basic configuration of proposed high step-up TI-SEPIC converter topology.

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Primary concern when using a tapped inductor is the discharge of the leakage inductance into the main switch, which results in an increased voltage spike and ringing across the switch. Hence, protection circuits should be employed. There are several possibilities. For instance Fig. 2 (a) illustrates a common RCD clamp [18] which can successfully limit the peak switch voltage across the switch. However, the circuit inflicts losses and impairs the efficiency. A better candidate is the nondissipative LCDD snubber [19], shown in Fig. 2 (b), or its inductorless versions [20], [21]. These snubbers can provide zero voltage switching, limit the peak voltage and recycle the captured energy back to the hold-up capacitor, C_1. However, this snubber requires additional inductive element, L_S. Finally, the prototype converter was fitted with "inductorless" regenerative snubber as shown in Fig. 2 (c). The snubber is comprised only of C_S, D_{S1} and D_{S2} and is a modification of the previous art [22], [23]. A hidden feature of the proposed snubber circuit in Fig. 2 (c) is that the tapped inductor's secondary leakage inductance is exploited as a part of the snubber discharge circuit. A closer look at Fig. 2 (c) reveals that during conduction of the switch, Q, the current of the charge pump diode D_1 can flow through the snubber diodes D_{S1} and D_{S2} instead. Hence, D_1 can be eliminated from the circuit. This simplifies the hardware and reduces the cost. Thus, the configuration in Fig. 2 (c) is regarded as a preferred solution and was investigated in detail in the course of this study.

The proposed topology possesses an additional merit. When the switch, Q, is turned on, the charge pump capacitor, C_1, clamps the anode voltage of the output diode, D_o, to ground. Hence, the voltage stress of D_o is independent of the tapped inductor turns ratio and equals the output voltage. This alleviates the switching losses of D_o and is an advantage of the proposed converter.

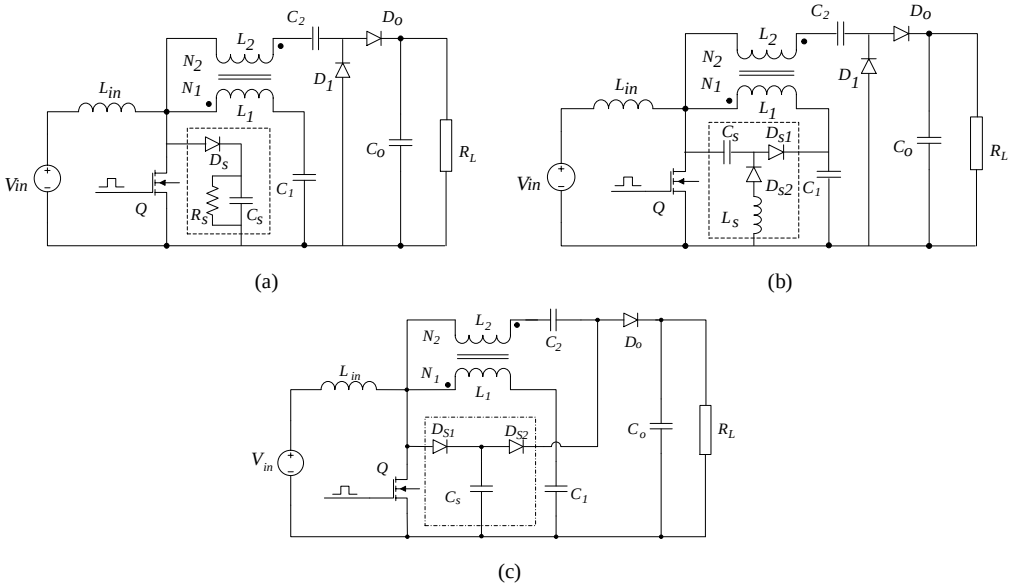

Fig. 2. Variants of the proposed high step-up TI-SEPIC converter topology with passive snubbers: (a) with RCD clamp; (b) with nondissipative LCDD snubber; (c) with "inductorless" regenerative snubber.

III. Modeling and Analysis

Schematic diagram of the proposed converter with the tapped inductor model and adopted convention of circuit variables is shown in Fig. 3. The proposed converter circuit is comprised of an input inductor, L_{in}; a main switch Q; an output diode D_o; an output filter capacitor C_o, a buffer capacitor C_1, and a charge pump capacitor C_2. The input voltage, the input current, and the load are designated as V_{in}, I_{in} and R_L respectively. The tapped inductor has a primary referred magnetizing inductance L_m, and a primary and a secondary leakage inductances L_{1k} and L_{2k}, respectively. The tapped inductor's turns ratio, n, is defined as:

$$n = N_2 / N_1 \qquad (1)$$

Here N_1 and N_2 are the primary and the secondary number of turns respectively.

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The "inductorless" regenerative snubber circuit, see Fig. 2 (c), consists of the snubber capacitor C_S and a pair of snubber diodes D_{S1} and D_{S2}. Instead of having an additional physical inductor, this snubber relies on the leakage inductances of the tapped inductor, L_{1k}, L_{2k} for proper operation.

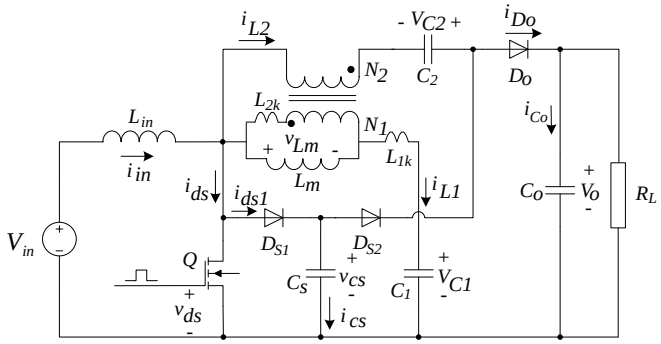

Fig. 3. Equivalent circuit of the proposed converter.

Analysis of the proposed converter is performed under several simplifying assumptions. The circuit components are assumed to be ideal. That is, the ON-state resistance of the main switch and of all the diodes, as well as their forward voltage drop and parasitic capacitances are neglected. At first approach the capacitors C_o, C_1, C_2, are considered sufficiently large and their respective voltages V_O, V_{C1}, V_{C2} can be assumed ripples. Also, the input inductor L_{in}, and the magnetizing inductance of the tapped inductor, L_m, are considered large, however, their current ripple will be taken into consideration.

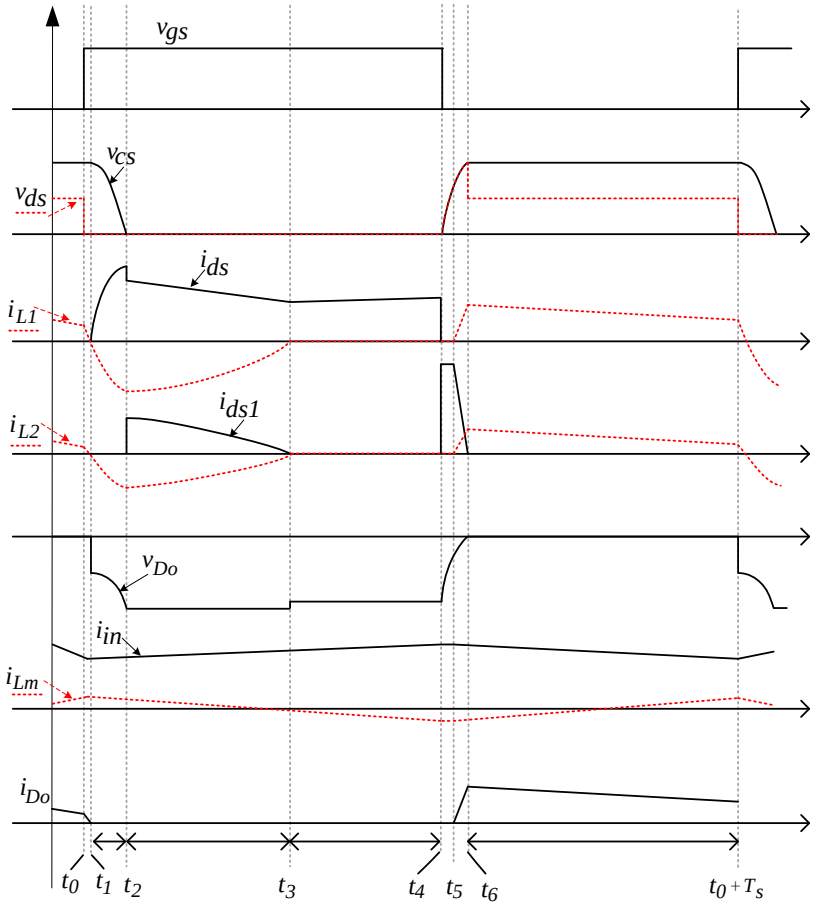

Fig. 4. Key waveforms of the proposed converter.

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The steady state waveforms of the proposed converter are shown in Fig. 4. Examination of the waveform reveals that the switching cycle of the proposed converter has seven distinct states. The equivalent circuits of the converter's states are shown in Fig. 5. Description of the states is given below.

A. State 1[t_0-t_1]

In this state, see Fig. 5 (a), the switch, Q, is turned on at $t=t_0$ and the switch voltage, v_{ds}, drops. Consequently, the input voltage, V_{in}, is applied across the inductor, L_{in}, and the input current, i_{in}, starts ramping up. The secondary leakage inductance keeps discharging the secondary current, i_{L2}, through D_O to the output. *State 1* is terminated as the secondary leakage current drops to zero. Since high output voltage is applied to the small leakage inductance duration of *State 1* is quite short.

B. State 2[t_1-t_2]

State 2 commences after the secondary current has decayed to zero and the output diode, D_O, has entered cut off, see Fig. 5 (b). Here, the snubber diode, D_{S2}, conducts and allows the snubber capacitor, C_S, to resonate with the secondary leakage inductance, L_{2k}, and dump the captured energy mostly into the charge pump capacitor, C_2. Thus, the secondary current, i_{L2}, reverses. This resonant current pulse is reflected to the primary of the tapped inductor and contributes to the switch current, i_{ds}. This state terminates as the snubber capacitor, C_S, is discharged and the voltage, v_{Cs}, drops to zero. Since $C_2>>C_s$, the equivalent characteristic impedance of the resonant circuit is determined by the reflected to secondary leakage inductances L_{1k}, L_{2k} and the snubber capacitor, C_S, and can be approximated as $Z_{0eq} = n\sqrt{(L_{1k} + L_{2k})/C_s}$. Hence, at the end of this state, the secondary current reaches the value, i_{L2max}, given by

$$i_{L2\max} = \frac{V_{ds\max}}{n}\sqrt{\frac{C_S}{L_{1k}+L_{2k}}} = \frac{V_{ds\max}}{Z_{0eq}}. \qquad (2)$$

The resonant cycle, $T_{CsEq,}$ is created by the reflected to secondary leakage inductances L_{1k} and L_{2k} of the tapped inductor and the equivalent capacitance of the series branch C_S-C_2. Since C_S dominates ($C_2 >>C_S$), the resonant cycle is

$$T_{CsEq} = n2\pi\sqrt{(L_{1k}+L_{2k})C_s}\ . \qquad (3)$$

Furthermore, the snubber capacitor, C_S, starts discharging from t_1 and gets fully discharged at the end of *State 2*. Thus, the duration of *State 2*, $\Delta t_2 = t_2 - t_1$ is about a quarter of a resonant cycle, T_{CsEq}, as shown below

$$\Delta t_2 \approx \frac{\pi}{2} n\sqrt{(L_{1k}+L_{2k})C_S} = \frac{1}{4}T_{CsEq}. \qquad (4)$$

C. State 3 [t_2-t_3]

State 3 commences after the snubber diode, D_{S1}, starts to conduct and clamps the snubber capacitor, C_S, to ground, see Fig. 4 and Fig. 5 (c). Here, the charge pump capacitor, C_2, keeps charging by resonant action with the reflected to secondary leakage inductances L_{1k} and L_{2k} so the equivalent resonant cycle is

$$T_{C2Eq} = n2\pi\sqrt{(L_{1k}+L_{2k})C_2}\ . \qquad (5)$$

The charging current, i_{L2}, reaches zero at $t=t_3$. Thus, the duration of *State 3*, $\Delta t_3 = t_3$-t_2, is somewhat shorter than a quarter of the equivalent resonant cycle T_{C2Eq}

$$\Delta t_3 \le \frac{1}{4}T_{C2Eq} = \frac{n\pi}{2}\sqrt{(L_{1k}+L_{2k})C_2}\ . \qquad (6)$$

At the end of *State 3*, at $t=t_3$, the charge pump capacitor C_2 is fully charged, the secondary resonant current pulse, i_{L2} , decays to

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zero, and, therefore, the diodes D_{S1} and D_{S2} are cut off at zero current.

D. State 4[t_3-t_4]

During *State 4* both the input inductor, L_{in}, and the magnetizing inductance of the tapped inductor, L_m, keeps charging linearly, see Fig. 5 (d). *State 4* lasts until the instant, $t=t_4$, here, the controller commands to terminate the on time and turns off the switch, Q.

E. State 5[t_4-t_5]

State 5 commences at $t=t_4$. After the switch Q is turned off, see Fig. 5 (e), the current of the central tap is diverted by the snubber diode D_{S1} towards the snubber capacitor, C_S, which moderates the rising of the switch voltage v_{ds}. Since the snubber capacitor voltage is zero at the start of the *State 5*, true Zero Voltage Switching (ZVS) performance is achieved. The current of the snubber capacitor, i_{Cs}, equals the sum of the input current, I_{in}, and the magnetizing current, I_{Lm} (i_{L1}), and may be approximated to a constant throughout this state.

Rising of the switch voltage, v_{ds}, causes the secondary tap voltage to rise. As a result, the output diode, D_o, cuts in at the instant $t=t_5$, then, *State 5* terminates. Because secondary current of the tapped inductor is zero during this state, leakage inductance can be neglected. Accordingly, the voltage across the snubber capacitor, C_S, at the end of *State 5* is

$$v_{CS(t_5)} = V_{C1} + V_{Lm(t_5)} = V_o - V_{C2} - nV_{Lm(t_5)} \tag{7}$$

After some manipulation, (7) yields the snubber capacitor voltage at the end of *State 5*

$$v_{cs(t_5)} = \frac{V_o - V_{C2} + nV_{C1}}{n+1} \tag{8}$$

F. State 6[t_5-t_6]

During *State 6*, see Fig. 5 (f), the snubber capacitor voltage, v_{Cs}, keeps rising while the secondary current builds up through the charge pump capacitor, C_2, and the output diode, D_o. *State 6* terminates as the snubber capacitor voltage reaches its peak value while the current falls to zero, at which instant diode D_{S1} cuts off. The equivalent circuit of the proposed converter in *state 6* is shown in Fig. 5 (g). Key equations for this state are:

$$\frac{L_{1k} + L_{2k}}{\left(1+\frac{1}{n}\right)^2}\frac{di_{L1}}{dt} = \frac{V_{in}}{1-D} - v_{Cs}, \tag{9}$$

$$C_S \frac{dv_{cs}}{dt} = -(I_{in(4)} - I_{Lm(4)}) - i_{L1}, \tag{10}$$

here, $I_{in(4)}$ and $I_{Lm(4)}$ are the input current and the primary current at $t=t_4$ respectively. Note, that till $t=t_5$ the magnitude of both of these currents is almost constant, see Fig. 4.

G. State 7[t_6-t_0]

During this state both the input inductance, L_{in}, and the magnetizing inductance, L_m, discharge to the output through the self transformer action of the tapped inductor. Inspection of Fig. 5 (h) reveals that the output voltage is the sum of the buffer capacitor voltage, V_{C1}, the charge pump capacitor voltage, V_{C2}, and (1+n) times v_{Lm} as follows

$$V_o = (1+n)v_{Lm} + V_{C1} + V_{C2}\ . \tag{11}$$

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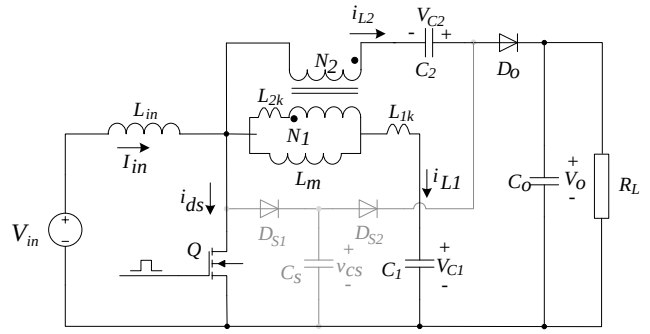

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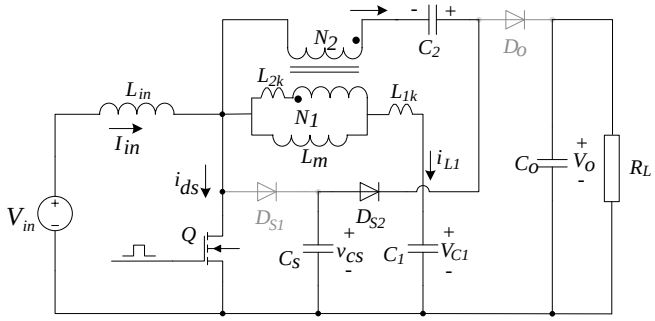

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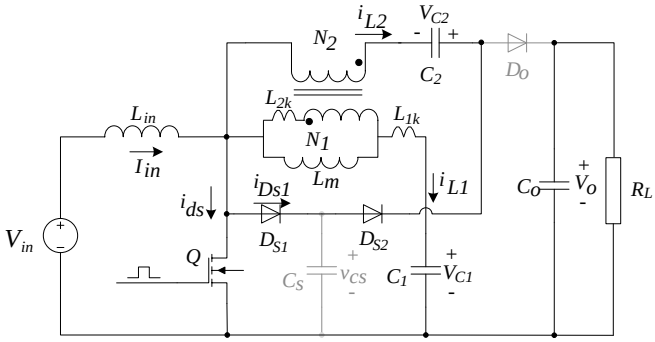

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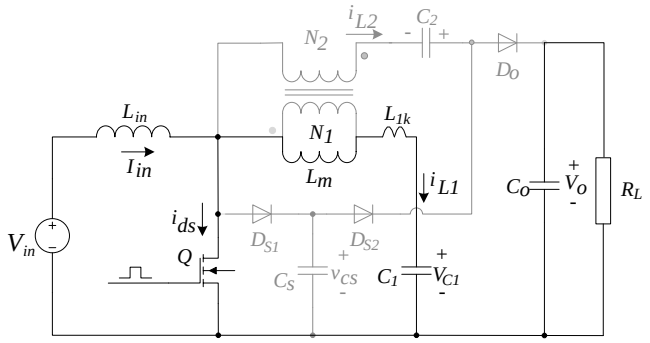

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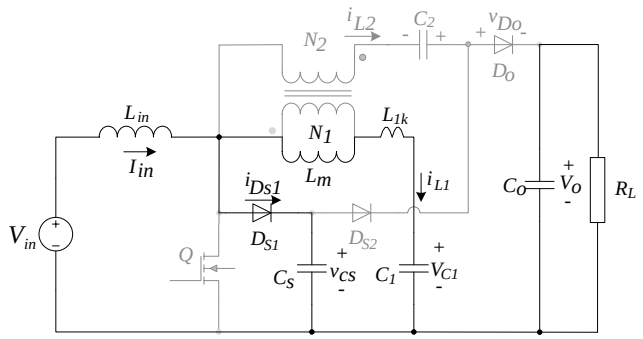

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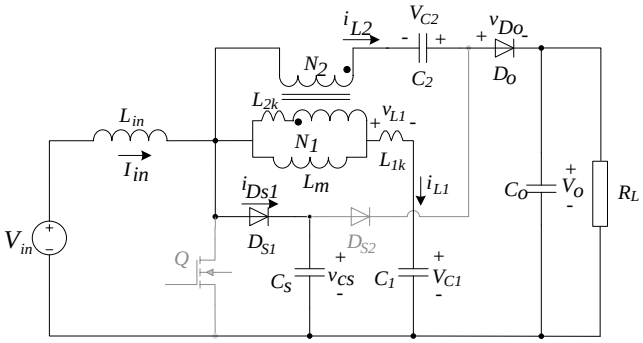

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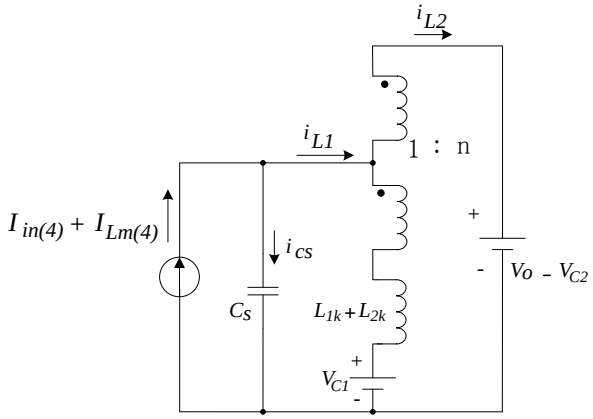

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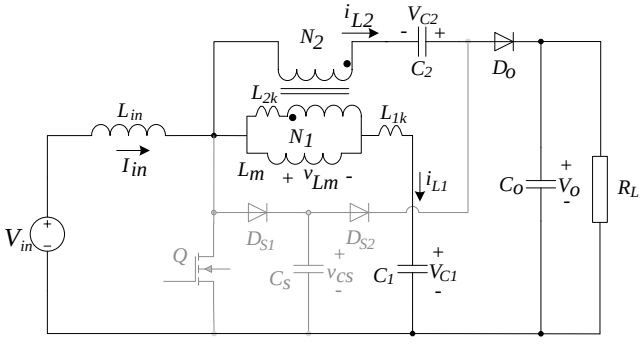

(h)

Fig. 5. Topological states of the proposed converter: *State 1* [t_0- t_1] (a); *State 2* [t_1- t_2] (b); *State 3* [t_2- t_3] (c); *State 4* [t_3- t_4] (d); *State 5* [t_4- t_5] (e); *State 6* [t_5- t_6] (f); equivalent circuit of State 6 (g); *State 7* [t_6- t_0] (h).

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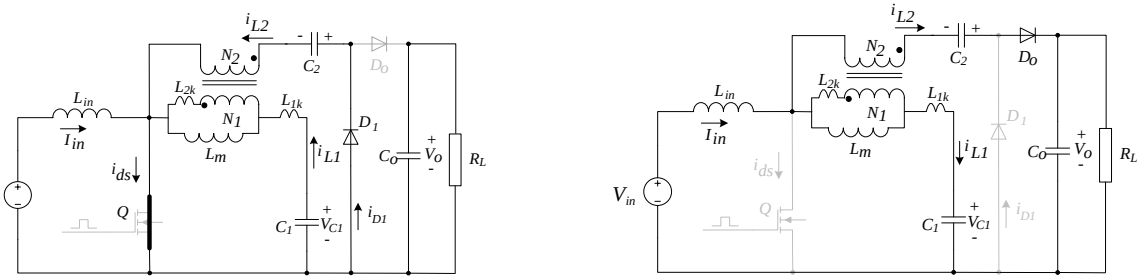
IV. Performance Analysis

A. Voltage and current conversion ratios

To facilitate the analysis approach, the ideal converter in Fig. 1 will be considered first. Here, it is also assumed that the voltage ripple across the capacitors C_O, C_1 and C_2 is negligible and their respective voltages V_O, V_{C1}, V_{C2} are constant. To further simplify matters, the coupling coefficient of the tapped inductor, k, is considered a unity **Error! Reference source not found.**, which allows neglecting the leakage inductances. The ideal converter in Fig. 1 has only two topological states illustrated in Fig. 6.



(a) (b)

Fig. 6. Key topological states of the idealized proposed converter of Fig. 1: Q_{on} sub topology (a); Q_{off} sub topology (b).

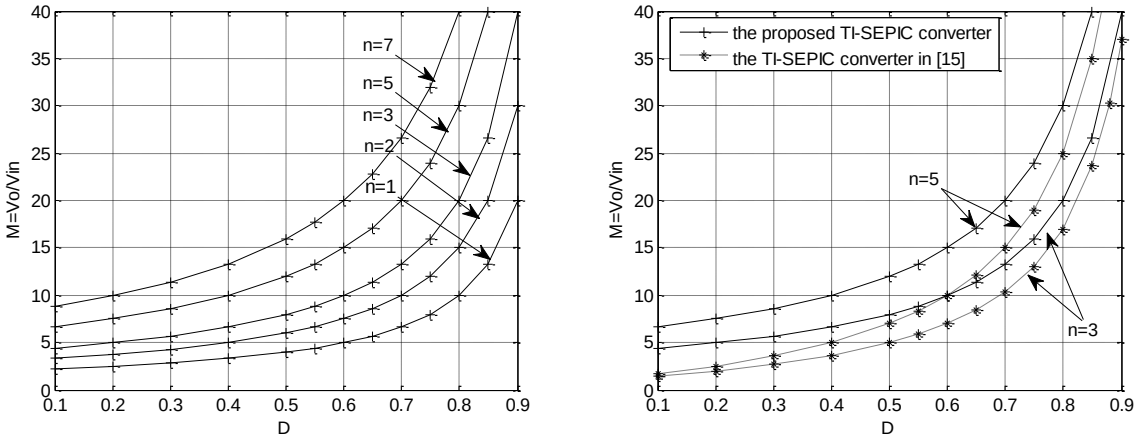
The conversion ratio of the idealized proposed converter in Fig. 1, in the CCM mode, is given by

$$M = \frac{V_o}{V_{in}} = \frac{1+n}{1-D}. \qquad (12)$$

See Appendix for details of derivation.

As shown below (Fig.11), the ideal conversion ratio (12) is sufficiently accurate and, therefore, is applicable to describe the chosen realistic topology in Fig. 2 (c). Hence, for sake of simplicity, (12) will be used throughout the following discussion.

The conversion ratio (12) of the proposed converter as function of the duty ratio, D, and tapped inductor turns ratio, n, is illustrated in Fig. 7 (a), which indicates that high voltage gain, M, can be achieved with a moderate turns ratio, n, avoiding the penalty associated with extreme duty ratio, D. For instance, voltage gain $M=10$ can be obtained with turns ratio $n=3$ and duty ratio $D=0.6$. Comparison of the voltage conversion ratio (12) of the proposed converter and an earlier TI-SEPIC converter **Error! Reference source not found.** is shown in Fig. 7 (b). Clearly, within the practical range of the duty cycle, D, the gain of the proposed TI-SEPIC converter is appreciably higher.



(a) (b)

Fig. 7. Voltage conversion ratio, M, of the proposed converter as function of the duty ratio, D, and the tapped inductor turns ratio $n=N_2/N_1$ of the proposed TI-SEPIC converter (a); Comparison with the TI-SEPIC converter in **Error! Reference source not found.** for $n=3, 5$ (b).

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The current conversion ratio, I_o/I_{in}, can be derived from (12) applying power balance considerations as

$$\frac{I_o}{I_{in}} = \frac{1-D}{1+n}. \quad (13)$$

B. Current Ripple and CCM conditions

a) Current Ripple Considerations

Examining the waveforms in Fig. 4 allows finding the peak input current ripple

$$\Delta I_{in} = \frac{DV_{in}}{2 f_s L_{in}}, \quad (14)$$

And the peak magnetizing current ripple

$$\Delta I_{Lm} = \frac{DV_{in}}{2 f_s L_m}, \quad (15)$$

According to Fig. 4 both I_{in} and I_{Lm} peak at $t=t_4$, hence, using (13), (14) and (15)the peak input current is

$$I_{in\max} = I_{in(4)} = I_{in} + \Delta I_{in} = MI_o + \frac{DV_{in}}{2L_{in} f_s}, \quad (16)$$

and, since the magnetizing current has zero average, at $t=t_4$ it reaches its peak negative value

$$I_{Lm\min} = I_{Lm(4)} = I_{Lm} - \Delta I_{Lm} \approx -\frac{DV_{in}}{2L_m f_s}. \quad (17)$$

These results will be used below.

b) Input CCM Condition

To ensure continuous conduction mode (CCM) of the input inductor requires $I_{inmin}>0$ throughout the switching cycle. Applying (14) and considering (12) and (13) yields

$$I_{in\min} = I_{in} - \Delta I_{in} = \left(\frac{1+n}{1-D}\right)^2 \frac{V_{in}}{R_L} - \frac{DV_{in}}{2L_{in} f_s} > 0, \quad (18)$$

Further manipulation of (18), leads to the CCM condition

$$K_{Lin} > K_{crit}(n, D), \quad (19)$$

where

$$K_{Lin} = 2L_{in} / R_L T_S, \quad (20)$$

and

$$K_{crit}(n, D) = D(1-D)^2 / (1+n)^2. \quad (21)$$

The dependence of $K_{crit}(n,D)$ on the duty cycle D at different turns ratio, n, is plotted in Fig. 8.

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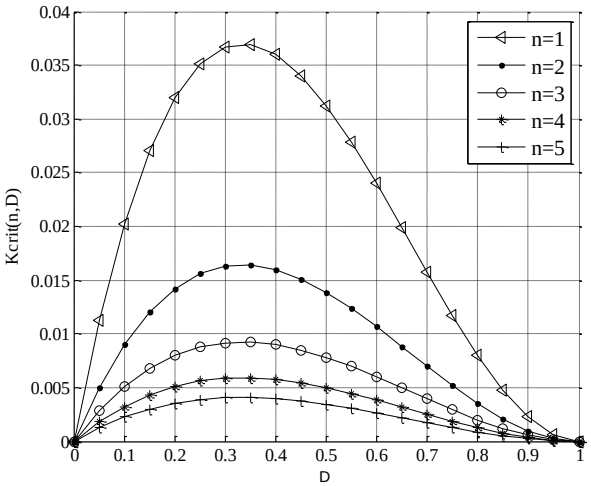

Fig. 8. Plot of the input current CCM - DCM boundary for selected turns ratio, *n*. CCM prevails for $K_{Lin}>K_{crit}(n,D)$.

c) Output CCM Condition

The CCM condition of the output diode, D_o, requires a non-vanishing current $I_{Do}>0$ throughout the switch off time. This implies, see Fig. 5 (g), that

$$(1+n)i_{Do} = i_{in} - i_{Lm} > I_{in\min} - I_{Lm\max} > 0\,. \tag{22}$$

Applying (14) and (15), equation (22) can be rewritten as

$$I_{in} - \Delta I_{in} - \Delta I_{Lm} = \left(\frac{1+n}{1-D}\right)^2 \frac{V_{in}}{R_L} - \frac{DV_{in}}{2L_{in}f_s} - \frac{DV_{in}}{2L_m f_s} > 0\,. \tag{23}$$

Introducing the definition

$$K_{Lm} = 2L_m/(R_L T_S)\,, \tag{24}$$

helps rewriting (23) as

$$1/\left(\frac{1}{K_{Lm}} + \frac{1}{K_{Lin}}\right) > K_{crit}(n,D)\,. \tag{25}$$

Hence, the constrain on inductor ratio, *h*, defined by

$$h = L_{in}/L_m = K_{Lin}/K_{Lm}\,, \tag{26}$$

can be derived combining (25) and (26) as

$$h > \frac{K_{Lin}}{K_{crit}} - 1\ , \tag{27}$$

When condition (27) is satisfied a non-vanishing current of the output diode, D_o, throughout the switch off time is attained.

C. Voltage Ripple Analysis

a) Output Capacitor Voltage Ripple

During the switch on time, the load is fully powered by the output filter capacitor, C_o. Therefore, the peak normalized output voltage ripple can be approximated to

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$$\frac{\Delta V_{Co}}{V_{Co}} = \frac{1}{2}\frac{\Delta Q_{CO}}{C_o} = \frac{I_o D T_s}{2C_o} \ . \tag{28}$$

b) Buffer Capacitor Voltage Ripple

The normalized peak voltage ripple across the buffer capacitor can be found as

$$\frac{\Delta V_{C1}}{V_{C1}} = \frac{1}{2}\frac{\Delta Q_{C1}}{V_{in}C_1} = \frac{1}{2}\left[\frac{n(1-D)}{(1+n)f_S}\frac{I_{in}}{V_{in}} - \frac{C_S}{C_1}\frac{V_{ds}}{V_{in}}\right]. \tag{29}$$

Details of derivation are given in the appendix.

Since the snubber capacitor is much smaller than the buffer capacitor, $C_S << C_1$, the second term in (29) can be neglected. Hence

$$\frac{\Delta V_{C1}}{V_{C1}} \approx \frac{n(1-D)}{2(1+n)f_S}\frac{I_{in}}{V_{in}} . \tag{30}$$

c) Charge Pump Capacitor Voltage Ripple

During the switch off time, the charge pump capacitor, C_2, resupplies the output with the charge drawn by the load, ΔQ_{C2}, see Fig. 4. Therefore, the normalized peak voltage ripple across the charge pump capacitor, C_2, is

$$\frac{\Delta V_{C2}}{V_{C2}} = \frac{1}{2}\frac{\Delta Q_{C2}}{nV_{in}C_2} = \frac{1}{2nf_sC_2}\frac{I_o}{V_{in}} . \tag{31}$$

Details of derivation are given in the appendix.

D. Stress Analysis

The predicted semiconductor's voltage and current stresses are summarized in Table I. The details of derivation are given in the appendix.

TABLE I
SUMMARY OF SEMICONDUCTORS' VOLTAGE AND CURRENT STRESSES (CCM)

Component	Performance Index
Switch Q	$V_{ds\max} = \frac{V_{in}}{1-D} + \left[I_{in} + \frac{DV_{in}}{2(n+1)f_S}\left(\frac{1}{L_{in}} + \frac{1}{L_m}\right)\right]Z_{0eq}$
	$I_{ds\max} = 2I_{in} + V_o / Z_{0eq}$
	$I_{dsrms} = \sqrt{I_{in}^2 D\left[1 + \frac{1}{3}\frac{(\Delta I_{in} + \Delta I_{Lm})^2}{I_{in}^2}\right] + \frac{V_{ds\max}^2}{8T_s Z_{0eq}^2}\left[T_{C2Eq} + (n+1)^2 T_{CsEq}\right]}$
Diode D_{S1}	$V_{Ds1max} = V_{dsmax}$
	$I_{ds1rms} = \sqrt{\frac{T_{C2Eq}}{8T_s}\left(\frac{V_{ds\max}}{Z_{0eq}}\right)^2 + \frac{C_S V_{in}}{(1-d)T_s}(I_{in} + \Delta I_{in} + \Delta I_{Lm}) + \frac{T_{CsEq}}{4T_s}(I_{in} + \Delta I_{in} + \Delta I_{Lm})^2}$
Diode D_{S2}	$V_{ds2\max} = nV_{in} / (1-D)$
	$I_{ds2rms} = \sqrt{(T_{C2Eq} + T_{CsEq})V_{ds\max}^2 / (8T_s Z_{0eq}^2)}$
Diode Do	$V_{Domax} = V_o$
	$I_{Dorms} = \frac{I_{in}}{(n+1)}\sqrt{(1-D)\left[1 + \frac{(\Delta I_{in} + \Delta I_{Lm})^2}{3I_{in}^2}\right]}$

E. Duty Cycle constrain

During *States 1,* and *States 2*, the energy captured earlier by the snubber capacitor C_S is transferred to C_2. Then, during *State 3* the

charge pump continues charging. Therefore, in order to complete this series of events properly, the switch on time, DT_s, should be greater than a certain minimum on time, $D_{min}T_s$, determined mainly by the duration of *State 2* and *State 3*

$$D_{\min}T_s = \Delta t_2 + \Delta t_3 , \qquad (32)$$

here, the duration of *State 1* was neglected.

Substitute (4) and (6), into (32) yields the minimum duty cycle D_{min} constrain

$$D_{\min} = \frac{1}{4} f_s (T_{CsEq} + T_{C2Eq}) . \qquad (33)$$

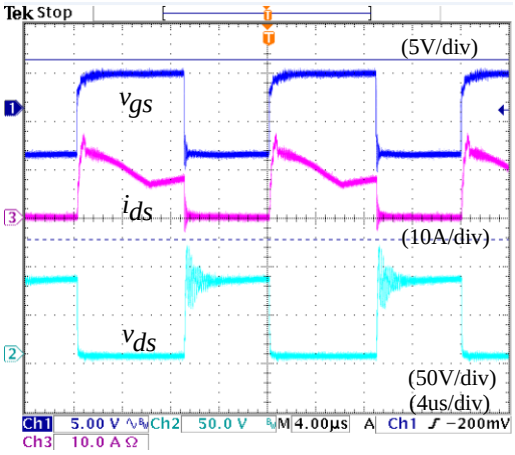
The minimum duty cycle, D_{min}, estimated by (33) is a worst case scenario. The reason is that the duration of *State 3*, Δt_3, approximated by (6) is over estimated, whereas, in practice, the circuit requires less time to complete *State 3*.

V. Experimental Results

To verify the theoretical predictions, a 200W, 35V-input 380V-output high step up TI SEPIC experimental prototype shown in Fig. 2 (c) was built and tested. The circuit parameters are listed below:

Switching frequency is f_s = 60 *kHz;* magnetizing inductance of the tapped inductor is L_m = 104 μH*;* and its turns ratio is N_1:N_2 = 16:64*;* the leakage inductance in primary side are estimated as 1μH (about 1% of the magnetizing inductance). The secondary leakage inductance referred to the primary side was also 1μH. Additional parameters were: the input inductor: L_{in} = 120 μH (the DCM/CCM boundary condition is 50% of P_{max})*;* capacitors: C_S = 10 *nF* /400V; C_1 = 10 μ *F* /100V; C_2 = 1 μF/400V; C_o= 47 μ *F* /600V. Semiconductor devices were: switch: *Q*: IRFB4332 (250V, $R_{DS(on)}$ =29 mΩ); Diodes: D_{S1} : STT3R02 (200V/16 ns); D_O and D_{S2} : C3D04065A (650V/8.5 nC/1.2 V).

The waveforms of the switch *Q* in experimental prototype are shown in Fig. 9. And the waveforms of diode, D_o, D_{S1} and D_{S2} are shown in Fig. 10. It shows that no voltage overshoot and no ringing were observed in voltage across the output diode, V_{Do}. Comparison of the simulated, experimentally measured and the theoretically predicted conversion ratio $M=V_o/V_{in}$ is shown in Fig. 11 and reveals that the theoretical expectation stands in good agreement with experimental results. Comparison of the simulated, experimentally measured and the theoretically predicted V_{dsmax} and I_{dsmax} is shown in Table II.



(a)

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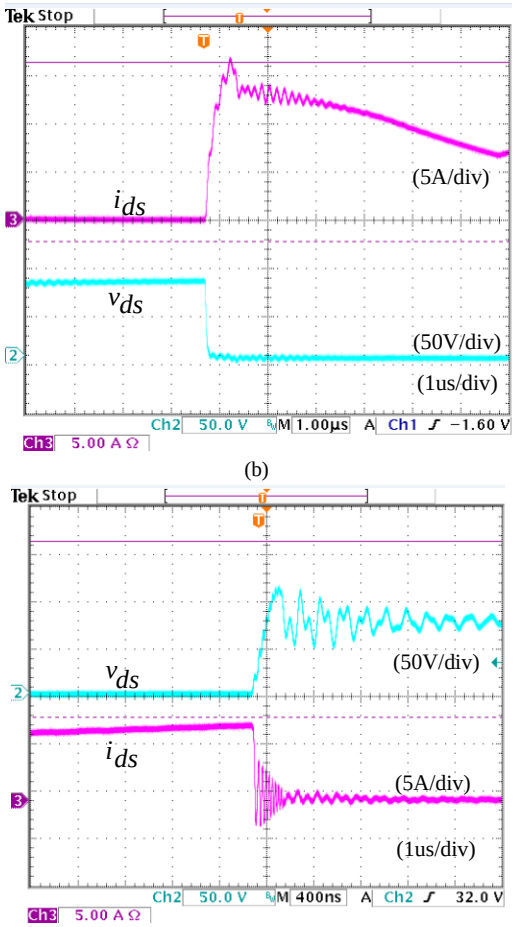
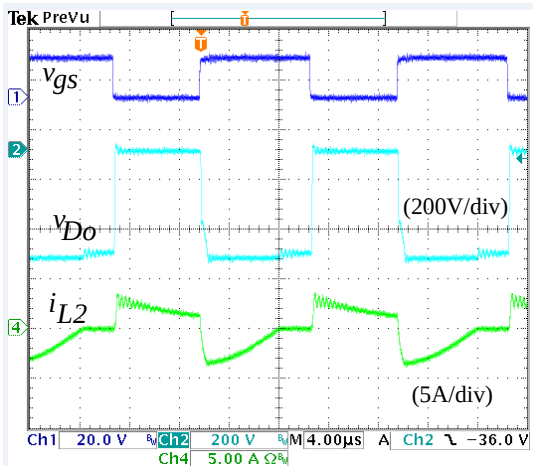


Fig. 9. Experimental results: measured switch voltage, v_{ds}, and current, i_{ds}, at full power P_o= 200W, full voltage V_o =380V conditions. (a) A general view of v_{gs}, v_{ds}, i_{ds}; (b) zero current switching at turn on of the switch; (c) zero voltage switching at turn off of the switch.



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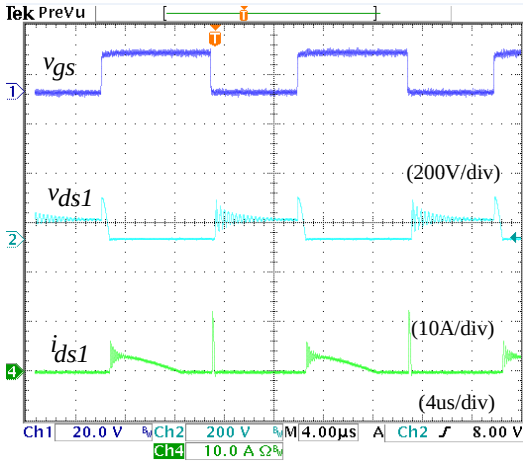

Fig. 10. Experimental results at full power P_o= 200W, full voltage V_o =380V conditions: (a) output diode voltage, v_{Do}, and secondary current of tapped inductor, i_{L2}; (b) current and voltage of snubber diode D_{S1}, i_{ds1},v_{ds1}; (c) current and voltage of snubber diode D_{S2}, i_{ds2},v_{ds2}.

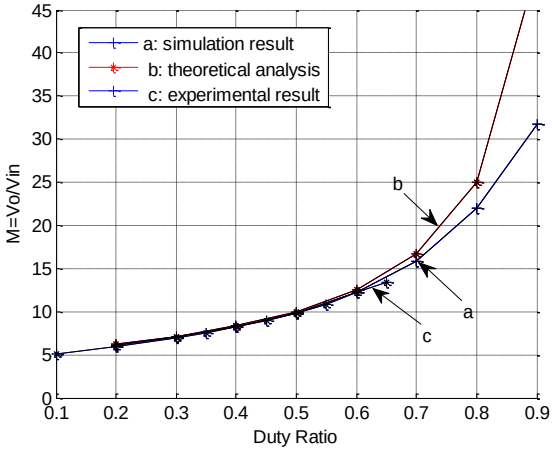

Fig. 11. Comparison of the simulated, experimentally measured and the theoretically predicted conversion ratio $M=V_o/V_{in}$.

TABLE II
COMPARISON OF THE SIMULATED, THE THEORETICALLY PREDICTED AND EXPERIMENTALLY MEASURED V_{dsmax} AND I_{dsmax}.

Power	Vdsmax (V)			Idsmax (A)		
	Sim.	Theory	Exp.	Sim.	Theory	Exp.
25%	107.3	114.5	98	9.85	11.35	8.9
50%	118.7	127.3	105	11.8	14.21	12.6
100%	147.7	153	120	19.34	19.92	17.2

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The efficiency of the prototype circuits as function of output power is shown in Fig. 12. Two different measurement approaches are compared. By first method the input power was found measuring the input current using a resistive current shunt and the input voltage was measured by a voltmeter. The results are shown in Fig. 12 (a). By the second approach Yokogawa digital power meter WT1600 was used, see Fig. 12 (b). Peak efficiency of 98.2% was measured using resistive shunt and voltage meter, whereas 95.8% peak efficiency was measured with Yokogawa power meter WT 1600. The results in Fig. 12 (a) and Fig. 12 (b) differ by approximately 2%. To compare the performance of the proposed snubber the experimental prototype was fitted with RCD snubber as in Fig. 2 (a) (Cs=1uF, Rs=2kOhm). Efficiency comparison shown in Fig.12 (c) clearly demonstrates the advantage of the proposed "inductorless" regenerative snubber. At low power range, the conduction losses are relatively low and the reduced switching loss improves the efficiency by 5-7%, whereas at high power level, as the conduction losses increase, the proposed snubber improves the efficiency by about 2-3%.

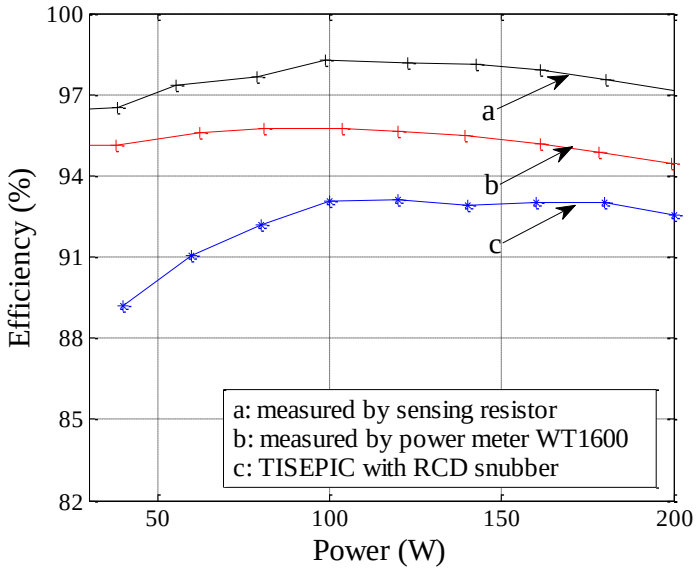

Fig. 12. Efficiency [%] as function of power level, at V_{in}=35, V_o=380V: (a) as measured by sensing resistor and voltage meter method; (b) as measured with Yokogawa power meter WT 1600, (c) efficiency of TI-SEPIC with RCD snubber in Fig.2 (a).

VI. Design Guidelines and Design Example

One possible design approach of the proposed converter is suggested below. In the given example the proposed converter is designed to attain the following specifications: rated power P_{omax} =200W; input voltage V_{in} = 35 *Vdc*; output voltage V_O = 380 *Vdc*; switching frequency f_S =60 kHz; the normalized peak output voltage ripple $k_{Co}=\Delta V_o/V_o$=0.01 (1%); the normalized peak voltage ripple across the buffer capacitor, C_1, $k_{C1}=\Delta V_{C1}/V_{C1}$=0.05 (5%); and normalized peak voltage ripple across the charge pump capacitor, C_2, $k_{C2}=\Delta V_{C2}/V_{C2}$=0.05 (5%). The design will attempt to employ a switch with rated V_{dsmax} =250V.

A. *Tapped Inductor Turns Ratio*

The conversion ratio (12) of the proposed converter depends on the duty cycle, *D*, and the turns ratio of the tapped inductor, *n*. Initially, Fig. 7 can be helpful to approximately select a favorable pair of parameters *n* and *D* that can provide the desired conversion ratio, *M*. It is easier to fabricate a tapped inductor with an integer turns ratio, hence, *n*, is selected first, then, a better estimation of the converter's duty cycle can be derived using (12) as

$$D = 1 - \frac{1+n}{M}. \qquad (34)$$

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For an initial choice of $n=4$, and applying (34), the required by the given specifications conversion ratio $M=V_o/V_{in}=10$ can be attained at moderate duty cycle $D=0.5$.

B. The input inductance, Lin, and magnetizing inductance, Lm,

In order to choose the value of the input inductor, L_{in}, the CCM-DCM borderline will be designed at $P_{ccm}= P_{omax}/3$. Either (21) or design chart in Fig. 8 can be used to establish the value of K_{crit}. In this design example to attain the desired M=10 turns ratio n=4 and duty cycle D=0.54 were chosen earlier. Hence, according to Fig. 8, the maximum K_{crit_max}=0.005, and according to (19), (21), , (24), (27), the minimum value of the inductance, L_{m_min}, can be obtained as

$$L_m < L_{m\_\min} = \frac{K_{crit\_\max}(h+1)V_o^2}{2 f_s P_{CCM}}. \qquad (35)$$

Next, considering (26) the minimum value of the input inductance, L_{in_min}, can be found

$$L_{in} < L_{in\_\min} = L_{m\_\min} / h \qquad (36)$$

According to (35) and (36), for $h=1$, L_m equals L_{in}. Hence, choosing $h=1$ in this design example leads to $L_m=L_{in}$=180uH.

C. The buffer capacitor C_1

To keep the voltage ripple of the buffer capacitor within the specified range, k_{C1}, requires

$$k_{C1} \geq \frac{\Delta V_{C1}}{V_{C1}} = \frac{\Delta V_{C1}}{V_{in}}. \qquad (37)$$

Substitution of (29) into (37), results in

$$k_{C1} \geq \frac{n(1-D) I_{in} T_s}{(n+1) V_{in} C_1} - \frac{C_s}{C_1(1-D)} \qquad (38)$$

Since $C_S << C_1$, the second term in (38) can be neglected and the value of the buffer capacitance, C_1, can be selected according to

$$C_1 \geq C_{1\min} = \frac{n(1-D) I_{in}}{(n+1) V_{in} k_{C1} f_s} \qquad (39)$$

For this design example, (39) yields the minimum buffer capacitance, $C_{1min}=20.03uF$.

D. The output filter capacitor C_o

To keep the voltage ripple of the output filter capacitor within the specified range, k_{Co}, it is required that

$$k_{co} \geq \frac{\Delta V_{CO}}{V_{CO}} \qquad (40)$$

Consequently, the minimum value of the output capacitor, C_{omin}, that satisfies the specifications on the peak output voltage ripple, k_{Co}, can be found from (28) and (39). Thus, the actual output capacitor value, C_o, should be chosen according to

$$C_o \geq C_{o\min} = \frac{I_o D}{k_{co} V_o f_s} \qquad (41)$$

Substituting the given above specs into (41) yields the value of the minimum output capacitance, $C_{omin}=1.06\mu F$.

E. The charge pump capacitor C_2

To keep the voltage ripple of the output filter capacitor within the specified range, k_{C2}, requires

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$$k_{C2} \geq \frac{\Delta V_{C2}}{V_{C2}}. \qquad (42)$$

Substituting (31) into (42) and considering (48), the minimum value of the charge pump capacitor needed to attain a specified voltage ripple across C_2 can be found according to

$$C_2 \geq C_{2\min} = \frac{I_o}{nV_{in} f_s k_{C2}} \ . \qquad (43)$$

Choosing a low value of the charge pump capacitor, C_2, that is, as closer to C_{2min} as possible, has the advantages of decreased circulating current and associated losses as well as makes the charging transients faster and helps meeting the duty cycle constrain (33).

Plugging the specifications of the design example into (43) results in $C_{2min}=1.253\mu F$.

F. Snubber capacitor C_s

Leaving some margin for transients, the peak voltage across the switch, V_{ds}, should be lower than about 75% of the maximum value of the selected component drain-source voltage, V_{dsmax} (250V). Therefore, according to(56)in appendix, the following condition should hold

$$\frac{V_{in}}{1-D} + \left[I_{in} + \frac{DV_{in}}{2 f_s}\left(\frac{1}{L_{in}} + \frac{1}{L_m}\right)\right]\left(\frac{Z_{0eq}}{n+1}\right) \leq 0.75V_{dsMAX} \qquad (44)$$

Hence, the estimated value of the snubber capacitor, C_S, can be obtained from (44) as

$$C_S \geq \frac{L_{1k} + L_{2k}}{\left(0.75V_{dsMAX} - \frac{V_{in}}{1-D}\right)^2}\left[I_{in} + \frac{DV_{in}}{2 f_s}\left(\frac{1}{L_{in}} + \frac{1}{L_m}\right)\right]^2 \left(\frac{n}{n+1}\right)^2 \qquad (45)$$

For a first pass design the primary and secondary leakage inductances can be approximated by $L_{1k}=L_{2k}=0.01L_m$ for a well coupled inductor. More accurate result can be obtained substituting measured parameters of a real device. For the given example, $C_S=10.3nF$.

Circuit parameters obtained by the outlined above design procedure are summarized in Table III. Converter performance was validated by simulation. Comparison of the targeted specifications and the resultant simulated performance indexes is shown in Table IV. Good agreement is found.

TABLE III
DESIGN EXAMPLE: SUMMARY OF CONVERTER'S PARAMETERS

n	L_{in}	L_m	C_1	C_2	C_O	C_S
4	180uH	180uH	20.03uf	1.253uf	1.06uf	10.3nf

TABLE IV
DESIGN EXAMPLE: COMPARISON OF THE SPECIFIED VS. SIMULATED PERFORMANCE INDEXES (P_{max}=200W)

	$V_o(V)$	D	$P_{CCM}/ Pmax$	k_{C1}	k_{C2}	k_{CO}	V_{dsmax}/ V_{dsMAX}
Specified	380.0	0.539	0.33	0.050	0.050	0.010	0.750
Simulated	380.8	0.535	0.29	0.051	0.045	0.012	0.731

VII. DISCUSSION AND COMPARISON WITH EARLIER COUNTERPARTS

The proposed topology, see Fig. 2 (c), resembles the earlier counterpart [33], illustrated in Fig. 13. However, further analysis reveals that the two circuits are different in their origins and, as a result, in their performance. Key distinction in between these two

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circuits is in the intended function and, accordingly, the value of only a single component. Yet, this forces the circuit to operate in a different regime and makes quite a difference.

The earlier circuit in Fig. 13 is, in fact, a boost derived converter. Here, the diode D_2 is the boost output diode and C_1 is a large boost output capacitor, in order of several μF, which holds a stiff boosted voltage. By its principle of operation, circuit in Fig. 13 cannot function as intended with D_2 and C_1 removed or replaced by other sub circuit. Whereas, the proposed topology in Fig. 2 (c) is SEPIC derived converter and applies D_{S1}, D_{S2}, and C_S, merely as a snubber. Here, C_S is a small, in order of a few nF, snubber capacitor which is fully charged and discharged and, therefore, experiences high voltage variations during a switching cycle. The proposed circuit can operate as intended and maintain its voltage conversion ratio (12) properly with any other snubber as well, see Fig. 2 (a) and Fig. 2 (b).

Furthermore, the switch in the earlier circuit in Fig. 13 operates with hard turn-off. This converter relies on clamping action of the boost capacitor in order to capture the leakage energy and limit the switch voltage stress. Whereas the snubber action in the proposed topology in Fig. 2 (c) attains lossless zero voltage turn-off and can limit the peak switch voltage according to the selected value of the snubber capacitor, see (56). However, with somewhat increased peak switch voltage due to higher swing of the snubber capacitor voltage, see Fig. 4.

Moreover, the multiplier cell used in [33], see Fig. 13, is charged by the voltage difference between the boost output and the voltage of the secondary winding and attains conversion ratio $M=(2+nD)/(1-D)$. Whereas, the charge pump in the proposed topology, see Fig. 2, is designed to be charged only by the voltage of the secondary winding and, therefore, the conversion ratio of the proposed converter is $M=(1+nD)/(1-D)$.

The efficiency of both converters is about equal. This can be explained by the fact that the proposed topology has higher peak switch voltage. This necessitates using a MOSFET with higher V_{dsmax} and R_{dson} values. Consequently, at moderate switching frequency, the advantage of the ZV turn-off is offset by higher switch conduction losses.

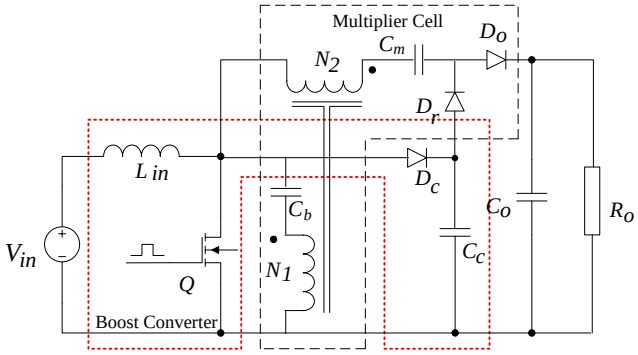

Fig. 13. Prior art: Single switch high step-up converter with built-in transformer voltage multiplier cell [33].

TABLE V
COMPARISON OF SELECTED TI-BASED HIGH GAIN DC/DC TOPOLOGIES (FOR n =4, D=0.5)

Topology No.	Total Part count	Switch count	Diode count	Inductor count	Capacitor count	Clamp/ Snubber	Soft-switching	Voltage Gain	Continuous input current
Proposed topology	11	1	3	2	4	Snubber	ZVS & ZCS	10	Yes
Ref[11]	6	1	2	1	2	Clamp	ZCS	6	No
Ref[14]	9	1	3	2	3	Snubber	ZVS & ZCS	5	No
Ref [15]	9	1	2	2	4	Clamp	ZCS	6	Yes
Ref [16]	8	1	3	1	3	Clamp	ZCS	10	No
Ref [24]	9	2	2	1	4	Clamp	ZCS	10	No
Ref [26]	11	1	4	1	5	Clamp	ZCS	14	No
Ref [31]	15	1	6	1	7	Clamp	ZCS	22	No
Ref [32]	13	1	5	2	5	Clamp	ZCS	24	Yes

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Table V presents a comparison of the proposed topology with a number of recently reported TI-based topologies considering several key features as comparison criteria. The voltage gain was calculated assuming ideal tapped inductor with zero leakage, and a moderate turns ratio, n= 4. Duty ratio of D=0.5 was assumed. As shown in table V, the proposed topology achieves high gain, continuous input current, ZVS and ZCS switching conditions while having moderate part count. Compared to some simpler high efficiency and high gain topologies like [15], the proposed topology offers better performance with regard to either gain or switching conditions.

VIII. Conclusion

This paper introduces a SEPIC derived converter, which integrates a tapped inductor and charge pump techniques. A passive regenerative snubber is incorporated into the design and contributes to low voltage stress and zero switching loss. Furthermore, the voltage across the rectifier diode is limited to the output voltage, which results in a reduced voltage stress of the device. For these reasons the proposed converter is a viable alternative for implementing renewable energy conversion systems, such as photovoltaic and fuel cell applications.

The paper described principles of operation and presented detailed analysis, design guidelines, simulation and experimental results obtained from a 200W prototype. The experimental converter operated from 35V low voltage dc source, generated 380Vdc output with efficiency above 95% in a wide load range with peak efficiency of 95.8%. High gain, high efficiency and soft switching merits of the proposed converter were demonstrated experimentally. Good agreement was found between theoretical predictions, simulation and experimental results.

IX. Appendix

a) Calculation of the voltage conversion ratio

To determine the conversion ratio of the idealized proposed converter in the CCM mode it is sufficient to consider the voltage across the magnetizing inductance. For the interval DT_S, the switch, Q, is turned ON, see Fig. 6 (a), the voltage of the magnetizing inductance is

$$V_{Lm} = V_{C1} = V_{in}. \tag{46}$$

Whereas, during $D'T_s$, when the switch, Q, is OFF, see Fig. 6 (b), the voltage of the magnetizing inductance is:

$$V_{Lm}' = \frac{1}{n+1}(V_{C1} + V_{C2} - V_o). \tag{47}$$

Inspection of Fig. 6 (a) also reveals that the capacitor C_2 is charged to approximately

$$V_{C2} = nV_{C1}. \tag{48}$$

Substitute (46), (47), (48) into volt-sec balance of the magnetizing inductance equation and recalling that V_{C1} equals V_{in}, the ideal voltage gain of the proposed topology can be obtained as (12).

b) Calculation of Buffer Capacitor Voltage Ripple

During the off time the current of the buffer capacitor, C_1, i_{C1}, see Fig. 5 (e) ~ (h), can be expressed as

$$i_{C1} = i_{L1} = i_{in} - i_{L2} - i_{ds1} = i_{in} - i_{D_O} - i_{cs}. \tag{49}$$

Accordingly, the charge increment, ΔQ_{C1}, of the buffer capacitor, C_1, during the off time is

$$\Delta Q_{C1} = \Delta Q_{Iin} - \Delta Q_{C2} - \Delta Q_{CS}, \tag{50}$$

here, the charge increment due to the input current, i_{in}, ΔQ_{Iin}, is

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$$\Delta Q_{Iin} = (1-D)T_S I_{in}, \tag{51}$$

whereas the charge, ΔQ_{Cs}, captured by the snubber capacitor, C_S, is

$$\Delta Q_{CS} = C_S V_{ds\max}, \tag{52}$$

The charge increment, ΔQ_{C2}, transferred during the off state by the output current, i_{Do}, to the output filter capacitor, C_o, equals the total charge drawn by the load current, I_o, throughout the switching cycle

$$\Delta Q_{C2} = I_o T_s. \tag{53}$$

Substitution of (49), (52) and (53) into (50), and using (13), yields the normalized peak voltage ripple across the buffer capacitor

$$\frac{\Delta V_{C1}}{V_{C1}} = \frac{1}{2}\frac{\Delta Q_{C1}}{V_{in}C_1} = \frac{1}{2}\left[\frac{n(1-D)}{(1+n)f_S}\frac{I_{in}}{V_{in}} - \frac{C_S}{C_1}\frac{V_{ds}}{V_{in}}\right]. \tag{54}$$

c) Calculation of Switch Voltage Stress

According to the analysis above, the switch voltage, v_{ds}, is peaking at the end of *State 6* at $t=t_6$. Equations (9) and (10) can be used to derive the peak voltage across the main switch as below

$$V_{ds\max} = \frac{V_{in}}{1-D} + \left(I_{in\max} - I_{Lm\min}\right)\left(\frac{Z_{0eq}}{n+1}\right). \tag{55}$$

Comparison of the theoretically predicted, (55), and simulated peak switch voltage is shown in Fig. 14. Good agreement is found.

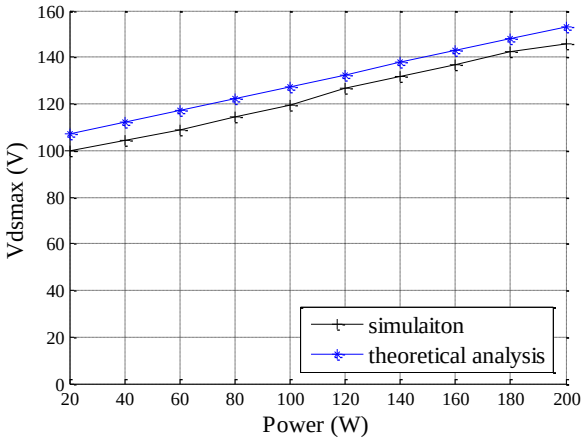

Fig. 14. Comparison of theoretically predicted and simulated peak switch voltage, *Vds_max* (for n=4, L_m=100uH, L_{in}=120uH, V_{in}=35V, V_O=380V).

Also applying (55), (16) and (17), the voltage stress of the main switch can be expressed in a normalized form as follows

$$\frac{V_{ds\max}}{V_{in}} = \frac{1}{1-D} + \left[\frac{I_{in}}{V_{in}} + \frac{D}{2f_s}\left(\frac{1}{L_{in}} + \frac{1}{L_m}\right)\right]\left(\frac{Z_{0eq}}{n+1}\right). \tag{56}$$

Note that the second term in (56) appears due to the leakage inductances, L_{1k}, L_{2k} and contributes to the voltage stress. Neglecting the leakage effect, that is assuming $Z_{0eq}=0$, the switch voltage stress can be roughly estimated using only the first term of (56) as

$$V_{ds\max} \approx \frac{V_{in}}{1-D} = \frac{V_o}{1+n}. \tag{57}$$

Equation (57) suggests that, in the ideal case, the peak switch voltage, V_{dsmax}, is much lower than the output voltage and can be alleviated by increasing the turns ratio, n. This is an advantage of the proposed circuit.

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d) Calculation of Switch Current Stress

The switch current is peaking at the end of the *State 2* at $t=t_2$, see Fig. 4. The expression of the switch peak current, I_{dsmax} , valid for CCM mode, can be derived as

$$I_{ds\max} = I_{in\_\min} - I_{Lm\_\max} + (1+n)i_{L2\max} . \quad (58)$$

Substitution of (2) into (58), and considering (14), (15)yields

$$I_{ds\max} = 2I_{in} + V_o / Z_{0eq} . \quad (59)$$

Equation (59) shows that the leakage inductances of the tapped inductor play an important role in limiting the peak current. Comparison of theoretically predicted (59) and simulation results are shown in Fig. 15. Good agreement is found.

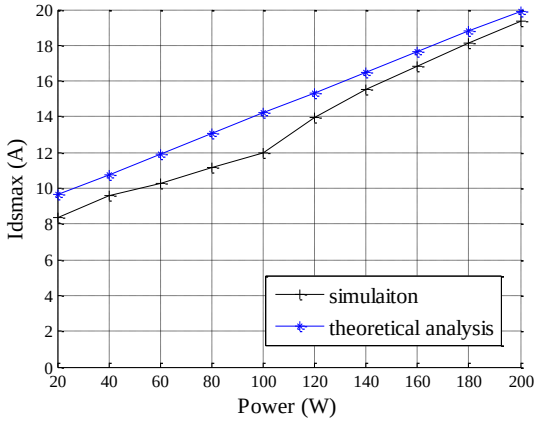

Fig. 15. Comparison of theoretically predicted and simulated I_{dsmax} as function of power (for n=4, L_m=100uH, L_{in}=120uH, L_{1k}=L_{2k}=1uH, V_{in}=35V, V_o=380V).

The switch current, see Fig. 4, can be thought of consisting of a trapezoidal pedestal, $i_{in}(t)$- $i_{Lm}(t)$, with superimposed sinusoidal fragments. Therefore, the rms switch current, I_{dsrms}, can be obtained according to

$$I_{dsrms} = \sqrt{\frac{1}{T_s}\left\{\int_0^{DT_s}\left[i_{in}(t)-i_{Lm}(t)\right]^2 dt + \int_{t_1}^{t_2}\left[(n+1)i_{L2}(t)\right]^2 dt + \int_{t_2}^{t_3}\left[ni_{L2}(t)\right]^2 dt\right\}} . \quad (60)$$

The term containing $\left[i_{in}(t)-i_{Lm}(t)\right]$ in (60) equals

$$\frac{1}{T_s}\int_0^{DT_s}\left[i_{in}(t)-i_{Lm}(t)\right]^2 dt = I_{in}^2 D\left[1+\frac{\left(\Delta I_{in}+\Delta I_{Lm}\right)^2}{3I_{in}^2}\right] . \quad (61)$$

An additional switch current component is the reflected discharge current of the snubber capacitance, C_S, which flows during *State 2*, $(t_1 - t_2)$. Here, the wave-shape of i_{L2} can be approximated to a quarter of sine having a resonant cycle T_{CsEq}, (3). Therefore, considering (2), this component contributes

$$\frac{1}{T_s}\int_{t_1}^{t_2}\left[(n+1)i_{L2}(t)\right]^2 dt = \frac{1}{4}\frac{T_{CsEq}}{T_s}\left[\frac{(n+1)i_{L2\max}}{\sqrt{2}}\right]^2 = \frac{T_{CsEq}}{8T_s}\left[\frac{(n+1)V_{ds\max}}{Z_{0eq}}\right]^2 . \quad (62)$$

Another switch current component is the reflected charging current of the charge pump capacitor, C_2, which flows during *State 3*, (t_2-t_3). Here, the wave-shape of i_{L2} can be approximated to a quarter of cosine having a resonant cycle T_{C2Eq}, see (6), this component contributes

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$$\frac{1}{T_s}\int_{t_2}^{t_3}\left[ni_{L2}(t)\right]^2 dt = \frac{1}{4}\frac{T_{C2Eq}}{T_s}\left(\frac{ni_{L2\max}}{\sqrt{2}}\right)^2 = \frac{T_{C2Eq}}{8T_s}\left(\frac{V_{ds\max}}{Z_{0eq}}\right)^2 . \quad (63)$$

Substitution of (61), (62) and (63) into (60), yields

$$I_{dsrms} = \sqrt{I_{in}^2 D\left[1+\frac{1}{3}\frac{\left(\Delta I_{in}+\Delta I_{Lm}\right)^2}{I_{in}^2}\right]+\frac{V_{ds\max}^{\ 2}}{8T_s Z_{0eq}^{\ 2}}\left[T_{C2Eq}+\left(n+1\right)^2 T_{CsEq}\right]} \quad (64)$$

The output diode current, i_{Do}, see Fig. 4, is

$$i_{Do} = \frac{1}{n+1}\left(I_{in}-I_{Lm}\right) \quad (65)$$

And, as mentioned above, $i_{in}(t)$- $i_{Lm}(t)$is of a trapezoidal shape. Therefore, considering (61) and (65), the *rms* current through the output diode, I_{Dorms}, is

$$I_{dorms} = \sqrt{\frac{1}{(n+1)^2 T_s}\int_{DT_s}^{T_s}\left[i_{in}(t)-i_{Lm}(t)\right]^2 dt} = \frac{I_{in}}{(n+1)}\sqrt{\left(1-D\right)\left[1+\frac{\left(\Delta I_{in}+\Delta I_{Lm}\right)^2}{3I_{in}^2}\right]} . \quad (66)$$

The snubber diode, D_{S2}, conducts during *States* 2 and *3*, as shown in Fig. 5 (b) and Fig. 5 (c). Thus, the *rms* current of D_{S2}, I_{ds2rms}, can be obtained using (62) and (63) as

$$I_{ds2rms} = \sqrt{\frac{1}{T_s}\int_{t_1}^{t_3} i_{L2}^2(t)dt} = \sqrt{\frac{\left(T_{C2Eq}+T_{CsEq}\right)}{8T_s}\left(\frac{V_{ds\max}}{Z_{0eq}}\right)^2} . \quad (67)$$

The snubber diode D_{S1} conducts during *States* 3, *5* and *6*, see Fig. 5 (c), (e) and (f). Therefore the *rms* current of D_{S1} can be obtained as

$$I_{ds1rms} = \sqrt{\frac{1}{T_s}\left[\int_{t_2}^{t_3} i_{Ds1}^2(t)dt+\int_{t_4}^{t_5} i_{Ds1}^2(t)dt+\int_{t_5}^{t_6} i_{Ds1}^2(t)dt\right]} . \quad (68)$$

In *State 3*, according to (63), there is

$$\int_{t_2}^{t_3} i_{ds1}^2(t)dt = \int_{t_2}^{t_3} i_{L2}^2(t)dt = \frac{T_{C2Eq}}{8}\left(\frac{V_{ds\max}}{Z_{0eq}}\right)^2 \quad (69)$$

Since during *State* 5, (t_4-t_5), see Fig. 5 (e), the current through the snubber diode D_{S1}, i_{Ds1}= I_{inmax} - I_{Lmmin}, the duration of *State* 5 can be found as ratio of snubber capacitance voltage divided by i_{Ds1}. According to (6), (48), and considering V_{C1} equals V_{in}, after some manipulation, yields

$$\int_{t_4}^{t_5} i_{ds1}^2(t)dt = \frac{C_S v_{CS(t_5)}}{\left(I_{in\max}-I_{Lm\min}\right)}(I_{in\max}-I_{Lm\min})^2 = \frac{C_S V_{in}\left(I_{in\max}-I_{Lm\min}\right)}{\left(1-D\right)} \quad (70)$$

Substituting (16) and (17) into (70), results in

$$\int_{t_4}^{t_5} i_{ds1}^2(t)dt = \frac{C_S V_{in}}{\left(1-D\right)}\left(I_{in}+\Delta I_{in}+\Delta I_{Lm}\right) \quad (71)$$

During *State 6*, (t_5-t_6), the current through diode D_{S1}, I_{ds1}, can be approximated to a quarter of a resonance cycle as described by (9) and (10), hence

$$\int_{t_5}^{t_6} i_{ds1}^2(t)dt = \frac{2\pi\sqrt{\left(L_p + L_s\right)C_s}}{4}\left(\frac{i_{Ds1\max}}{\sqrt{2}}\right)^2 = \frac{T_{CsEq}}{4}\left(I_{in} + \Delta I_{in} + \Delta I_{Lm}\right)^2 \quad (72)$$

Substitution of (69), (71) and (72) into (68), yields

$$I_{ds1rms} = \sqrt{\frac{T_{C2Eq}}{8T_s}\left(\frac{V_{ds\max}}{Z_{0eq}}\right)^2 + \frac{C_S V_{in}}{(1-d)T_s}\left(I_{in} + \Delta I_{in} + \Delta I_{Lm}\right) + \frac{T_{CsEq}}{4T_s}\left(I_{in} + \Delta I_{in} + \Delta I_{Lm}\right)^2} \quad (73)$$

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