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Secondary-Side Phase-Shift Controlled Dual-Transformer-Based Asymmetrical Dual-Bridge Converter With Wide Voltage Gain

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***Abstract*—A novel dual-transformer-based asymmetrical dual-bridge (DT-ADB) converter with secondary-side phase-shift control strategy is proposed. The primary-side of the DT-ADB converter is a fully active full-bridge, and the secondary-side is a semi-active bridge comprising of one active leg and two passive legs. The current and power of the two transformers in the converter are shared automatically by adopting primary-side-series and secondary-side-parallel configuration, and the turns ratio of the transformer is reduced by employing two transformers. The high-frequency-link inductor is reduced because the voltage applied on the inductor is reduced compared to previous converters, and hence the efficiency and power density can be improved. Zero-voltage turn-ON of all the active switches and zero-current turn-OFF of all the diodes is achieved in a wide operation range. Furthermore, the turn-OFF losses of the secondary side active switches are reduced because only half of the output current flows through the switches. Moreover, the proposed topology offers several other advantages including continuous output current and smaller output filter requirement. The operation principle is analyzed and experimental results are provided to verify the effectiveness and advantages of the proposed converter.**

***Index Terms*—DC-DC converter, soft switching, asymmetrical dual active bridge, secondary-side phase-shift**

I. Introduction

ISOLATED DC-DC converter is one of the main and most important parts for various power systems, such as the power supplies for telecommunications and computers, DC-DC stage of different types of photovoltaic inverters, and battery chargers in electric vehicles etc., to meet the requirements of galvanic isolation and voltage/current conversion ratio [1][2]. Besides, it is an emergent research topic to achieve high conversion efficiency in a wide input/output voltage range [3][4]. For example, the output voltage of the photovoltaic array may fluctuate by over 100% due to the change of environment conditions, and the battery voltage also varies in a wide range depending on the State of Charge.

To achieve high efficiency and power density, many soft-switching DC-DC converters have been proposed to overcome the disadvantages of hard-switching DC-DC converters [5]-[22]. Among them, the phase-shift full-bridge converter is widely used, especially in medium to high power applications, because it can achieve zero-voltage-switching (ZVS) for all the active switches by adopting phase-shift modulation. However, some of the disadvantages of the phase-shift full-bridge converter include high voltage ringing and reverse-recovery on the secondary side rectifier diodes, limited ZVS range, circulating current-related power loss and duty cycle loss. Large amount of work has been done to solve these problems [5]-[9]. Generally, some additional components need to be introduced to suppress the circulating currents and alleviate the reverse-recovery problem. For instance, an auxiliary inductor, transformer or active switch is introduced to reduce the circulating current in [5]-[8]. An advanced isolated DC-DC converter should be able to realize soft-switching for all the switching devices, not only the active devices but also the rectifying diodes. From this point of view, the LLC resonant converter is an attractive solution [10]. Soft-switching of all the active switches and rectifier diodes over a wide load range can be achieved with the LLC resonant converter by designing and selecting a proper operation region [11]-[13]. However, it is difficult to obtain a wide range of voltage regulation while maintaining high efficiency due to the large circulating current when the operating frequency is far from the resonant frequency. Some modified LLC converters are proposed to achieve high efficiency in a wide range of input or output voltages [14][15], but these converters involve adding many extra components, suffer from complex topology and control. The dual active bridge converter is a preferred topology for bidirectional isolation power conversion due to its many advantageous features with constant switching frequency [16]. But the ZVS range of the dual active bridge converter strongly dependent on the voltage conversion ratio and output power [17][18]. Besides, the root-mean-square currents through the transformer and semiconductor are relatively high due to circulating current. If the power flow is unidirectional, the dual active bridge converter can be improved to be a semi-dual active bridge converter with simplified topology and improved performance [19]-[22]. However, although zero voltage switching (ZVS) turn-ON of active switches and zero current switching (ZCS) of diodes are achieved, the turn-OFF

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losses of the secondary-side active-switches are relatively high. Another drawback of these converters is that the inductor size in these converters is relatively large owing to the application of voltage at the inductor with the applied volt-second increasing with the input and output voltages. In addition, the power cannot be transmitted to the load when the inductor is charged by the input voltage, which results in a discontinuous output current.

A secondary-side phase-shift (SSPS) controlled dual-transformer asymmetrical dual-bridge (DT-ADB) converter with reduced power losses, small high-frequency-link inductor, and continuous output current is proposed in this paper. The current and power of the two transformers are auto-balanced by adopting primary-side-series secondary-side-parallel configuration. ZVS of all the active switches and ZCS of all the diodes are achieved in a wide operation range. Moreover, the converter can work in three modes, including the buck, balance and boost modes, which mean the converter has a wide voltage conversion range. All the advantages make the proposed converter competitive in the high input voltage large output current and wide range conversion applications.

II. Proposed Converter and Operational Principle

A. Topology of the Proposed Converter

The proposed dual-transformer-based asymmetrical dual-bridge (DT-ADB) converter is shown in Fig. 1. The primary side of the DT-ADB converter is an active-bridge comprising of four MOSFETs, S_1~S_4, and the secondary-side is a semi-active-bridge comprising of one active leg, S_5&S_6, and two passive legs, D_1~D_4. The two active-bridges are connected by two transformers, T_1 and T_2, and a high-frequency-link inductor, L_f. The primary windings of the two transformers are in series. The secondary-side circuit is redrawn in Fig. 2 to show the connection clearly. It can be seen that, the active leg composed of S_5 and S_6 and the passive leg composed of D_1 and D_2 build a hybrid full-bridge rectifier for the transformer T_1, while the two passive legs on composed of D_1~D_4 build another full-bridge rectifier for the transformer T_2. The passive leg comprising of D_1 and D_2 is shared by the two full-bridge rectifiers. The output of the two full-bridge rectifiers are in-parallel. So, a primary-side-series and secondary-side-parallel configuration is adopted for the two transformers. The parameters of the two transformers are the same with each other, N_{P1}=N_{P2}=N_P and N_{S1}=N_{S2}=N_S. Since the primary windings of the two transformers are in-series, the current flows through the corresponding primary and secondary windings of the two transformers are always the same. The inductor L_f, which can be either implemented with the leakage inductance of the transformers or with an external inductor to achieve the desired value, is a key element in determining the power handling capacity and operation mode of the DT-ADB converter.

B. Operational Principle

All of the four primary switches and the two secondary switches have the constant duty cycle of 0.5. The switches S_1 and S_4 turns ON and OFF simultaneously, while the switches

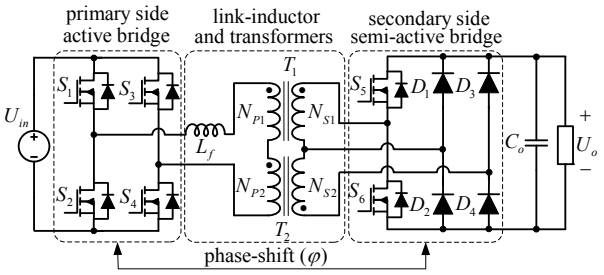

Fig. 1. Topology of the proposed dual-transformer-based asymmetrical dual-bridge converter.

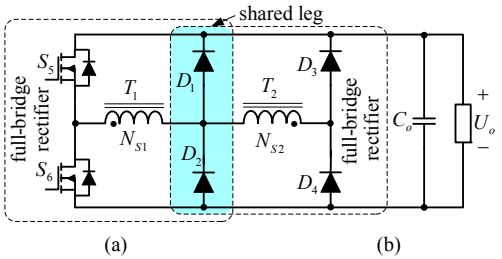

Fig. 2. Secondary side circuit of the DT-ADB converter.

S_2 and S_3 share the same gate signal. The phase-shift angle φ between the primary and secondary bridges is employed to control the output voltage and power.

According to the operation conditions of the primary current, the converter has three different operation modes, namely continuous current mode 1 (CCM1), continuous current mode 2 (CCM2), and discontinuous current mode (DCM), respectively. In order to simplify the analysis, the parasitic capacitance of MOSFETs is ignored, and the normalized voltage gain is defined as

$$G = \frac{2NU_o}{U_{in}} \tag{1}$$

where U_{in}, U_o and N are the input voltage, output voltage, and primary to secondary turns ratio of the transformers N_P:N_S, respectively. The converter can work in the buck mode (G<1), balance mode (G=1) or boost mode (G>1), and the current flowing through the high-frequency-link inductor L_f increases, keeps constant, and decreases at the main-power-transferring stage of the three modes, respectively. Because the phase shift angle serves the same function as duty cycle in PWM converter, we define equivalent phase shift duty cycle D

$$D = \frac{\varphi}{\pi} \tag{2}$$

1) CCM1 Mode

The key waveforms when the DT-ADB converter works in the CCM1 mode with voltage gain G>1 are shown in Fig. 3, where D_0 is defined as the equivalent duty cycle during which the primary current returns to zero after the primary side switches turn OFF, and T_S is the switching period. There are ten stages in one switching period. Due to the symmetry of the circuit, only five stages are analyzed and corresponding equivalent circuits for each operation stage are shown in Fig. 4.

Stage 1 [t_0, t_1] [see Fig. 4(a)]: Before t_0, primary switches S_2, S_3, secondary switch S_6 and diodes D_1 and D_4 are ON. At

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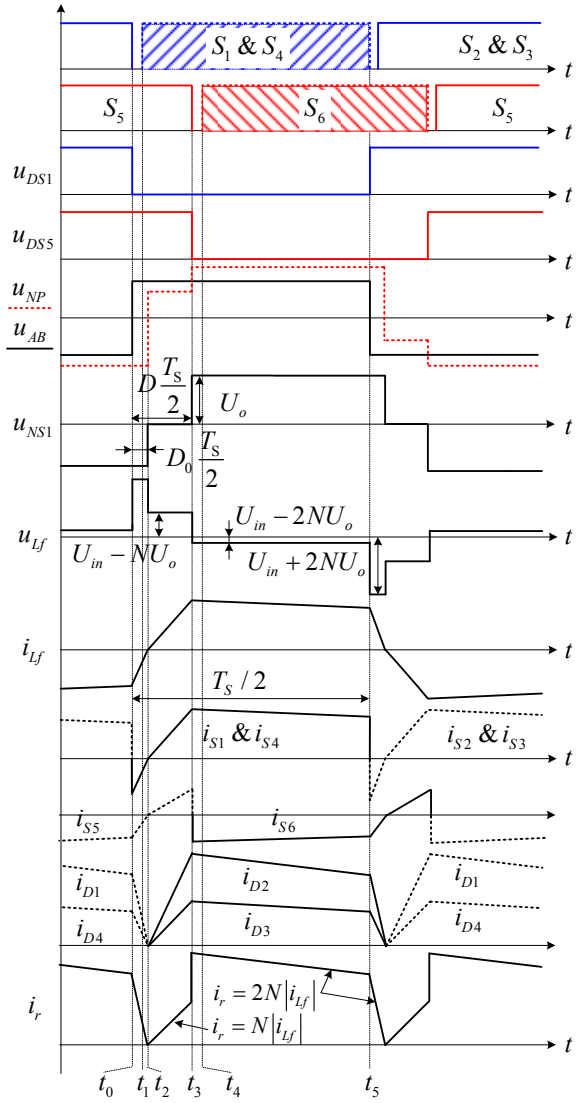

Fig. 3. Waveforms of CCM1 with voltage gain G>1.

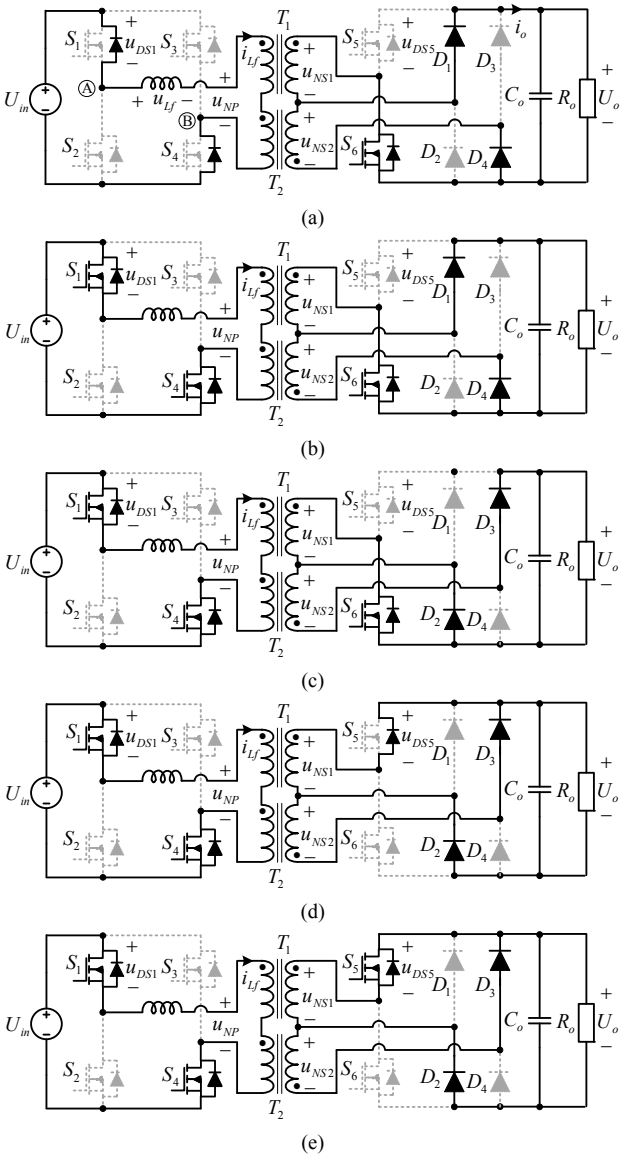

Fig. 4. Equivalent circuits in CCM1, (a) Stage 1 [t_0, t_1], (b) Stage 2 [t_1, t_2], (c) Stage 3 [t_2, t_3], (d) Stage 4 [t_3, t_4] and (e) Stage5 [t_4, t_5].

t_0, S_2 and S_3 turn OFF. During this interval, the inductor current i_{Lf} flows reversely through the body diodes of S_1 and S_4, which results in zero-voltage turn-ON of S_1 and S_4. The power is delivered from L_f to the input and the output side. The voltage applied to the inductor L_f is (U_{in}+2NU_o). Due to the negative voltage across the inductor, the current i_{Lf} decreases rapidly, which is expressed as

$$i_{Lf}(t) = i_{Lf}(t_0) + \frac{2NU_o}{L_f}\left(\frac{1}{G}+1\right)(t-t_0) \tag{3}$$

Stage 2 [t_1, t_2] [see Fig. 4(b)]: At t_1, S_1 and S_4 are turned ON with zero-voltage. i_{Lf} returns to zero at the end of this stage, and the rectified current i_r also reaches zero. The secondary diodes D_1 and D_4 are OFF naturally without reverse-recovery. Stage 1 and Stage 2 are the inductor current reset stage, in which the inductor current i_{Lf} is reset to zero. In the CCM1 mode, the equivalent duty cycle D_0 satisfies D_0<D.

Stage 3 [t_2, t_3] [see Fig. 4(c)]: At t_2, i_{Lf} reaches zero and starts increasing linearly. As i_{Lf} increases, the diodes $D_2$and D_3 on the secondary-side begins to conduct with current increasing from zero. The transformer T_1 is shorted by the switch S_6 and D_2, and will not transfer power to the load. In this stage, part of the total input power is charged to and stored in the inductor L_f, which is similar to a conventional boost converter, while the other part of the input power is transferred to the load through the transformer T_2. So, even when the high-frequency-link inductor L_f is charged by the input voltage, the power is still transferred to the load, which leads to a continuous output current. This is one of the improvements of the proposed DT-ADB converter compared with the previous semi-dual-active-bridge converter presented in [19]-[22]. For the previous converters, when the inductor is charged by the input voltage, there is no power transferred to the load, which leads to a discontinuous output current. On the other hand, for the proposed converter, it should be noted that, the voltage applied to the inductor L_f is (U_{in}-NU_o), thus, the current i_{Lf} is regulated by

$$i_{Lf}(t) = i_{Lf}(t_1) + \frac{NU_o}{L_f}\left(\frac{2}{G}-1\right)(t-t_1) \tag{4}$$

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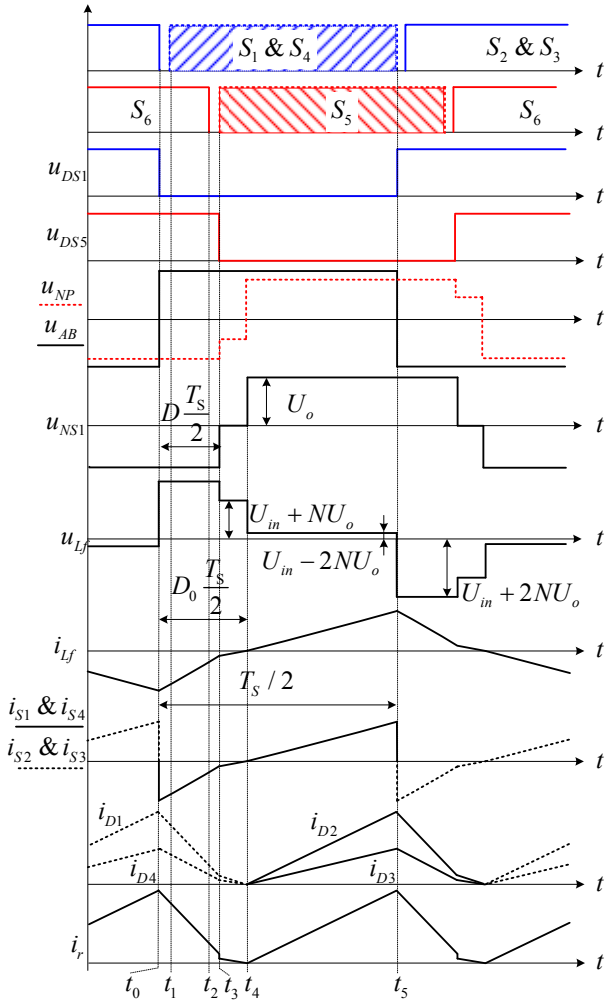

Fig. 5. Waveforms of CCM2 mode.

However, for the previous semi-dual-active-bridge converter, when the inductor is charged, the equivalent voltage applied to the inductor is U_{in} [19]-[20], which is much higher than that of the proposed converter. It means a much larger inductor is needed if the rate of change of the inductor current is the same as the proposed converter.

Stage 4 [t_3, t_4] [see Fig. 4(d)]: At t_3, S_6 turns OFF, the current flows through the body diode of S_5. So, the zero-voltage turn-ON of S_5 can be achieved naturally. It should be noted that, since only half of the current flows through the secondary winding of T_1, the turn-OFF current of S_6 is also halved compared to the previous converter [20], so the turn-OFF loss can also be reduced effectively.

Stage 5 [t_4, t_5] [see Fig. 4(e)]: At t_4, S_5 is turned-ON with zero-voltage.

During Stage 4 and Stage 5, both the two transformers deliver power from U_{in} to the load. Most of the power is transferred to the load during these two stages, which are named as the main-power-transferring stage. The inductor current can be calculated as

$$i_{Lf}(t)=i_{Lf}(t_3)+\frac{2NU_o}{L_f}\left(\frac{1}{G}-1\right)(t-t_3) \tag{5}$$

In the boost mode, G>1 and i_{Lf} decreases during this stage,

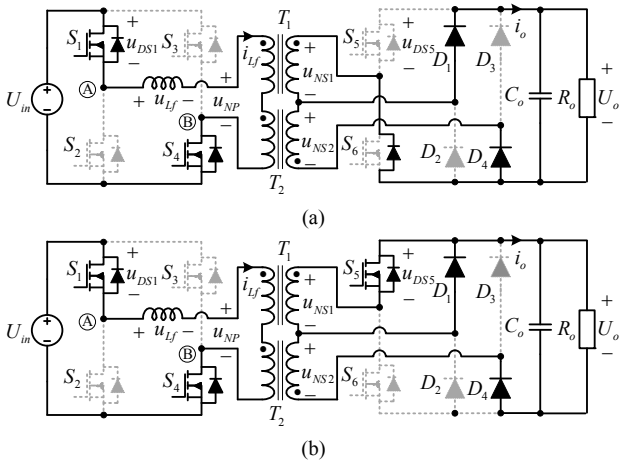

Fig. 6. Equivalent circuits in CCM2, (a) Stage 3 [t_2, t_3] and (b) Stage 4 [t_3, t_4].

as shown in Fig. 3. If the converter operates in the balance (G=1) or buck mode (G<1), i_{Lf} will keep constant or increase, respectively, during the main-power-transferring stage.

The main-power-transferring stage is ended when S_1 and S_4 are turned OFF. A similar operation works in the rest stages of a switching period. It should be noted that, since the two transformers are connected in-series on the primary-side, the current flows through the corresponding primary and secondary windings of the two transformers are always the same. However, only the transformer T_2 transfers power to the load in the Stage 3 while the transformer T_1 doesn't transfer power to the load. So, the transferred power of T_1 is lower than that of T_2.

2) CCM2 Mode

In the CCM1 mode, the equivalent phase-shift duty cycle, D, is greater than the equivalent current-reset duty cycle, D_0. However, if D<D_0, the converter will enter the CCM2 mode. The key waveforms when the converter works in the CCM2 mode are shown in Fig. 5. As shown in Fig. 5, the converter can only work in the buck mode with voltage gain G<1 in the CCM2 mode, because the voltage across the inductor must be positive in order to increase the inductor current during the main-power-transferring stage. There are also ten stages in one switching period of CCM2 mode. The main-power-transferring stage and the primary MOSFETs switching stages are similar to the CCM1 mode, while the main differences between the CCM1 and CCM2 modes can be observed in the secondary-side MOSFETs switching intervals.

Stage 1 [t_0, t_1], Stage 2 [t_1, t_2]: The operation principles and equivalent circuits of the two Stages are exactly the same as that of Stage 1 and Stage 2 in the CCM1 mode.

Stage 3 [t_2, t_3]: At t_2, before i_{Lf} returns to zero, S_6 is turned OFF. The current will flow through the body diode of S_6, instead of S_5. The equivalent circuit is shown in Fig. 6(a). As a result, zero-voltage-switching performance of the secondary side active switches will be lost in the CCM2 mode, but zero-current-switching of the diodes can also be achieved.

Stage 4 [t_3, t_4]: At t_3, S_5 is turned ON. The secondary winding of the transformer T_1 is shorted by S_5 and D_1, as shown in Fig. 6(b), so the inductor current in this stage can be given by

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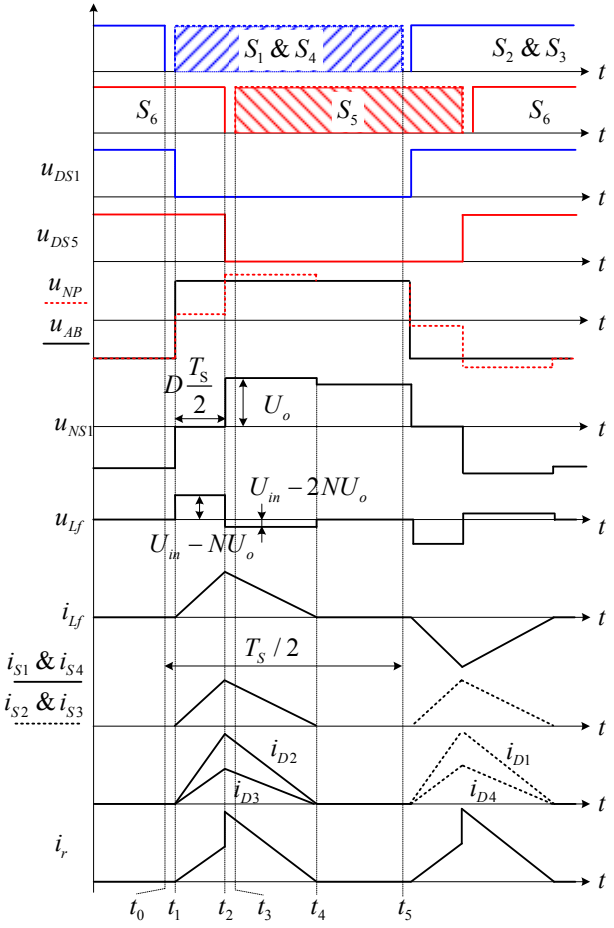

Fig.7. Waveforms of DCM mode.

$$i_{Lf}(t)=i_{Lf}(t_3)+\frac{NU_o}{L_f}(\frac{2}{G}-1)(t-t_3) \tag{6}$$

This stage ends when the inductor current i_{Lf} reaches zero, and also, the diodes D_1 and D_4 are OFF naturally without reverse-recovery.

Stage 5 [t_4, t_5]: The operation and equivalent circuit of this Stage are the same as that of Stage 5 in the CCM1 mode. After this stage, a similar operation works in the rest stages in a switching period.

3) DCM Mode

If the primary current has decreased to zero before the primary side switches commutate, the converter enters the DCM mode, in which the converter can only work in the boost mode. The key waveforms of the DT-ADB converter operating in DCM are shown in Fig. 7. There are also ten stages in one switching period. Due to the symmetry of the circuit, only five stages are analyzed here and corresponding equivalent circuits for each operation stage are shown in Fig. 8.

Stage 1 [t_0, t_1] [see Fig. 8(a)]: Before t_0, S_2, S_3 and S_6 are ON. Since i_{Lf}=0, there is no energy transferred from the input to the output. All the diodes are revise-biased. At t_0, S_2 and S_3 turn OFF with zero-voltage and zero-current.

Stage 2 [t_1, t_2]: At t_1, S_1 and S_4 are turned ON with zero-current. i_{Lf} begins to increases from zero. The operation principle and equivalent circuit of this stage are the same as

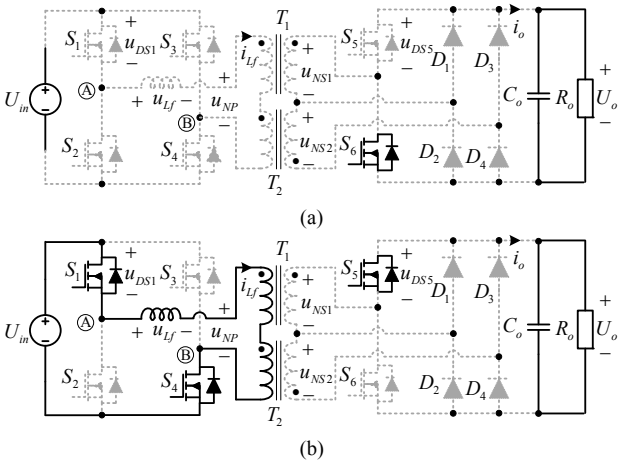

Fig. 8. Equivalent circuits in DCM, (a) Stage 1 [t_0, t_1], and (b) Stage5 [t_4, t_5].

the Stage 3 in CCM1 mode, in which part of the total in power is charged to and stored in the inductor L_f while the other part of the input power is transferred to the load through the transformer T_2.

Stage 3 [t_2, t_3], Stage 4 [t_3, t_4]: The operation principles and equivalent circuits of the two Stages are the same as that of Stage 4 and Stage 5 in the CCM1 mode.

Stage 5 [t_4, t_5] [see Fig. 8(b)]: At t_4, i_{Lf} reaches zero. The diodes D_2 and D_3 are OFF naturally with zero-current and without reverse-recovery. i_{Lf} will stay in zero state in this stage and there is no energy transferred from the input to the output. After t_5, a similar operation works in the rest stages of the switching period.

As shown in Fig. 7, i_{Lf} must keep decreasing linearly to zero at Stage 4. Therefore, the converter can only work in the boost mode for DCM with voltage gain G>1.

III. Performance Analysis

A. Output Characteristics

For simplification, the input and output power can be normalized to the following bases:

$$\begin{cases} P_{b1}=\dfrac{U_{in}^2}{2\pi f_s L_f} \\ P_{b2}=\dfrac{(2NU_o)^2}{2\pi f_s L_f} \end{cases} \tag{7}$$

where f_s is the switching frequency, and P_{b1}=G^2P_{b2}.

According to the operational analysis of the CCM1 mode, the average primary current can be given by:

$$I_{in}=\frac{i_{Lf}(t_0)}{2}D_0+\frac{i_{Lf}(t_3)}{2}(D-D_0)+\frac{i_{Lf}(t_3)+i_{Lf}(t_5)}{2}(1-D) \tag{8}$$

Ignoring the power losses, then, the output power can be derived as:

$$P_o=P_{in}=U_{in}I_{in} \tag{9}$$

From (1)~(5), and (7)~(9), the output power can be obtained as

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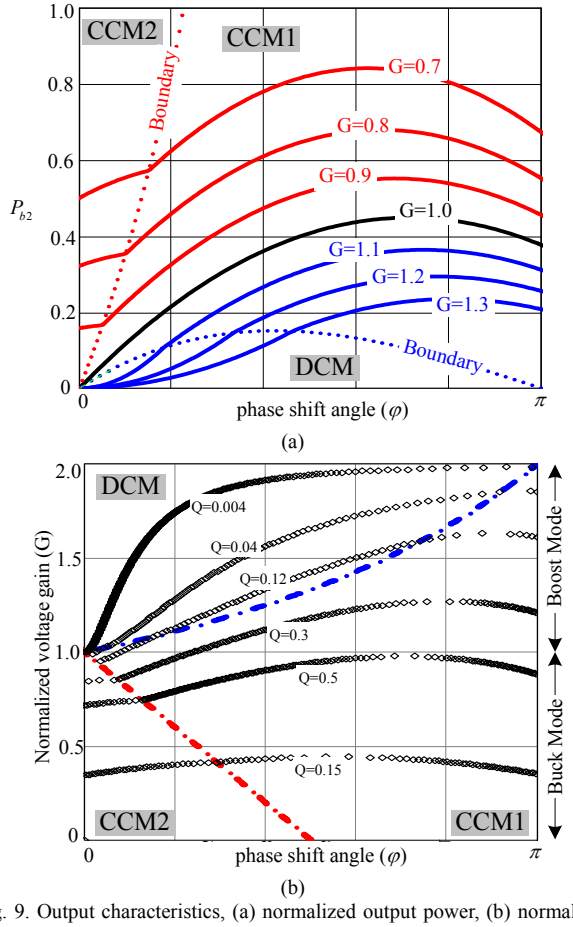

Fig. 9. Output characteristics, (a) normalized output power, (b) normalized voltage gain.

$$P_{o\_CCM1}(G,\varphi)=P_{b1}\frac{G}{2(4+G)^2}[3\pi(2+G-3G^2)+4\varphi(2+G+2G^2)$$
$$-2(4+2G+G^2)\frac{\varphi^2}{\pi}] \tag{10}$$

The same analysis process can be performed for CCM2 and DCM modes. The output power can be obtained as:

$$\begin{cases} P_{o\_CCM2}(G,\varphi)=P_{b1}\dfrac{G}{2(4-G)^2}[(3\pi+4\varphi)(2-G-G^2) \\ +2(-4+2G-G^2)\dfrac{\varphi^2}{\pi}] \\ P_{o\_DCM}(G,\varphi)=P_{b1}\dfrac{G(2-G)\varphi^2}{8\pi(G-1)} \end{cases} \tag{11}$$

At the boundary between CCM1 and CCM2, the phase-shift duty cycle, D, is equivalent to the current-reset duty cycle, D_0. In this scenario, based on the volt-second balance of the inductor L_f, the boundary condition can be derived as

$$\varphi_{B1}=(1-G)\frac{\pi}{2} \tag{12}$$

Similarly, the boundary condition between the DCM and CCM1 is determined by

$$\varphi_{B2}=\frac{(G-1)2\pi}{G} \tag{13}$$

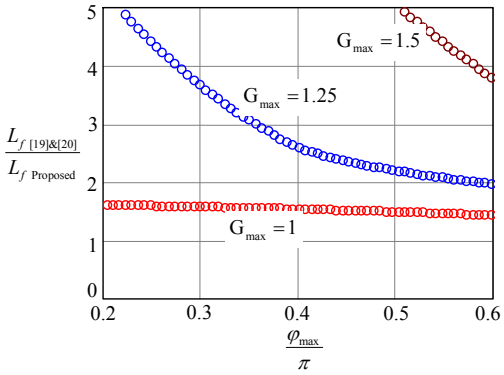

Fig. 10. Comparison of the high-frequency-link inductor.

Based on the analysis, the normalized output power curves versus the phase shift angle are plotted in Fig. 9(a), where the output power is normalized by P_{b2}. Fig. 9(b) is the curves of normalized voltage gain G versus the phase shift angle, where the characteristic factor is defined as

$$Q=\frac{\pi f_s L_f}{2N^2 R_o} \tag{14}$$

and R_o is the load resistance. It can be seen that, the proposed DT-ADB converter can operate in the buck mode with voltage gain range of 0~1, or in the boost mode with voltage gain range of 1~2. When the voltage gain is constant, the output power in the CCM1 mode is greater than DCM and CCM2 modes. Besides, CCM2 only occurs when the voltage gain G<1 while DCM only occurs when the voltage gain G>1, which agrees with the analysis in the previous section. Besides, it can be seen that the main operation region of the converter is the CCM1 mode, in which soft-switching performance can be achieved for all of the active switches and rectifying diodes.

B. High-Frequency-Link Inductor

The high-frequency-link inductor L_f is a key element in determining the power handling capacity of the proposed converter. According to Fig. 9, when the output voltage is determined, the maximum output power decreases with the increasing of voltage gain G or the decreasing of input voltage. Therefore, once the minimum input voltage $U_{in\min}$, maximum voltage gain G_{max} (G_{max}>1), maximum phase-shift angel φ_{max} and power capacity P_{omax} are determined, the value of L_f can be calculated according to (7) and (10)

$$L_f=\frac{U_{in\min}^2}{2\pi f_s P_{o\max}}\frac{G_{\max}}{2(4+G_{\max})^2}[3\pi(2+G_{\max}-3G_{\max}^2)$$
$$+4\varphi_{\max}(2+G_{\max}+2G_{\max}^2)-2(4+2G_{\max}+G_{\max}^2)\frac{\varphi_{\max}^2}{\pi}] \tag{15}$$

On the other hand, for the previous semi-dual-active-bridge converters, those presented in [19] and [20] and employ only one transformer and one semi-active-bridge, the desired high-frequency-link inductor L_f is calculated by

$$L_f=\frac{U_{in\min}^2}{2\pi f_s P_{o\max}}\frac{G_{\max}}{2(2+G_{\max})^2}[\pi(1+G_{\max}-2G_{\max}^2)$$
$$+4\varphi_{\max}(1+G_{\max}+G_{\max}^2)-2(2+2G_{\max}+G_{\max}^2)\frac{\varphi_{\max}^2}{\pi}] \tag{16}$$

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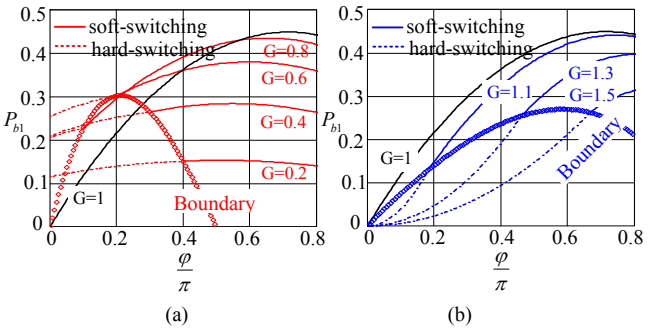

Fig. 11. Soft-switching range of (a) secondary-side switches, and (b) primary-side switches.

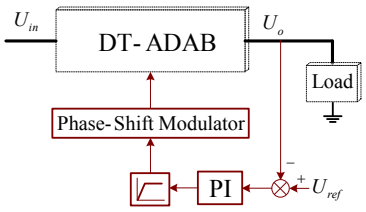

Fig. 12. Control block diagram.

According to (15) and (16), when the specifications of the proposed converter and the previous converters in [19] and [20] are the same, the comparison of the high-frequency-link inductors are shown in Fig. 10. It is obvious that, if the rated-power of these converters is the same, the desired high-frequency-link inductor of the previous converters is much larger than that of the DT-ADB converter. The ratio $L_{f[19]\&[20]}/L_{f\ \text{Proposed}}$ is proportional to the maximum voltage gain and reversely proportional to the maximum phase shift angle. Since the inductor can be reduced significantly with the proposed converter, the power losses related to the inductor is reduced. Hence, the efficiency and power density can be improved.

Although it is possible to use smaller inductor in the previous topologies and reduce the phase shift to get the same rated power at same inductor value as the proposed topology, according to Fig. 9(a), once the rated output power is given and the maximum output power is much larger than the rated power, the operation region of CCM2 and DCM modes will increase and the range of CCM1 mode will decrease, which will hurt the conversion efficiency and performance of the converter

C. Soft-Switching Performance

According to the operation principles, zero-current OFF of all of the diodes can be achieved in the whole operation range. Therefore, the reverse-recovery loss of the diodes can be fully eliminated with the proposed converter. However, for the previous semi-dual-active-bridge converters, zero-current OFF is lost when they operate in the CCM2 mode. This is another improvement of the proposed converter. Zero-voltage ON of the primary side switches can be achieved when the converter works in the CCM1 and CCM2 modes. Since the value of the high-frequency-link inductor is much larger than the drain-source capacitance of the switches, neglecting the small current required to charge/discharge the capacitances, the condition $\varphi>\varphi_{B2}$ ensures soft-switching of primary-side switches if the voltage gain $G>1$. Zero-voltage ON of the secondary side switches can be achieved in the CCM1 and DCM modes. Therefore, the condition $\varphi>\varphi_{B1}$ ensures soft-switching of secondary-side switches if the voltage gain $G<1$. The soft-switching ranges of secondary-side and primary-side switches are shown in Fig. 11(a) and (b), respectively. Besides, as illustrated in Fig. 9, the main operation mode of the converter is CCM1, which indicates that zero-voltage ON can be achieved for all the switches in a wide operation range. In addition, although the secondary-side switches are hard-switching in the CCM2 mode, the turn-OFF current is relatively small in this mode, as illustrated in Fig. 5. That means the switching loss of the secondary side switches in the CCM2 mode is not very high.

D. Control Loop

According to the output characteristic curves shown in Fig. 9, the output voltage and power can be regulated by varying the phase shift angle directly. Thus, the traditional voltage feedback loop can be adopted to regulate the output voltage, as shown in Fig. 12. The difference between the voltage reference and the sampled output voltage is used as the input of the PI regulator to generate the command value for the phase-shift modulator. Since the control loop is very simple, it can be implemented with either Analog Circuit or Digital Signal Processor.

As shown in Fig. 9, the output voltage and power are proportional with the phase-shift angle. Once the normalized voltage gain $G\geq1$ and the phase shift angle φ is larger than the boundary phase shift angle φ_{B2}, the converter operates in the CCM1 mode. When the output power decreases, the phase shift angle decrease as well, and once $\varphi<\varphi_{B2}$, the converter will enter the DCM mode. Once the normalized voltage gain $G<1$ and the phase shift angle φ is larger than the boundary phase shift angle φ_{B1}, the converter operates in the CCM1 mode, otherwise, the converter will enter the CCM1 mode.

E. Performance Comparison

Since the DT-ADB converter has a full-bridge input stage, the conventional phase-shift full-bridge converter and the full-bridge converters in [19] and [20] are selected for performance comparison due to the similarity in structure and application, while others may not be suitable for comparison and are out of the scope of this paper. Table I summarizes the findings from this investigation.

IV. Experimental Verifications

A. Verification of the Proposed Converter

A 1-kW 100k-Hz prototype is established to verify the theoretical analysis. The input voltage of the prototype is 400V, and the output voltage is 60V~80V. The transformer turns ration N is 2.8, which means the converter works in the balance mode at the output voltage of 72V ideally. The specifications are listed in Table II, and the picture of the prototype is shown in Fig. 13.

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TABLE I
PERFORMANCE COMPARISON

		DT-ADB	Phase-shift full-bridge	Converters in [19] and [20]
Total components used in the converters	Primary side power devices	4 MOSFETs	4 MOSFETs	4 MOSFETs
	Secondary side power devices	2 MOSFETs + 4 Diodes	4 Diodes	2 MOSFETs + 2 Diodes
	Inductors	1 (smaller than [19] and [20])	2 (1 for soft switching)	1
	Transformer	2 (small)	1 (large)	1 (large)
Voltage conversion ration	Boost conversion	Yes	No	Yes
	Buck conversion	Yes	Yes	Yes
Soft switching	Primary side devices	Yes	Yes	Yes
	Secondary side devices	Yes	No	Yes
Voltage stress	Primary side devices	U_{in}	U_{in}	U_{in}
	Secondary side devices	U_o	$>>U_o$	U_o
Power loss	Primary side	Low	Medium (circulating current)	Low
	Secondary side	Low (reduced turn off loss)	High (hard switching)	Medium
Modulation Strategy		Phase-shift (secondary side)	Phase-shift (Primary side)	Phase-shift (secondary side)
Cost		High	Low	Medium
Design effort		High	Low	High

TABLE II
COMPONENTS AND PARAMETERS OF THE PROTOTYPE

Components	Parameters
Input voltage (U_{in})	400V±10V
Output voltage (U_o)	60V~80V
Rated output power (P_o)	1000W
Switching frequency	100kHz
Turns ratio of transformer (N)	2.8
High-frequency link inductor (L_f)	60uH
Primary side MOSFETs	IPW60R299CP
Secondary side MOSFETs	IRFB33N15D
Secondary side diodes	V30100SG
Output capacitors (C_o)	330uF

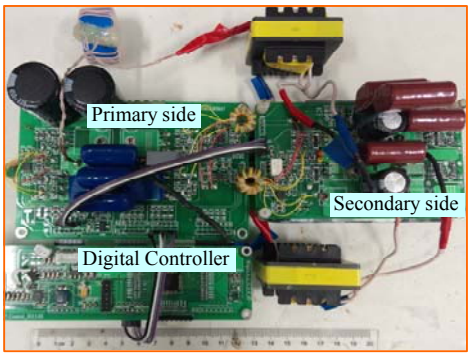

Fig. 13. Experimental prototype.

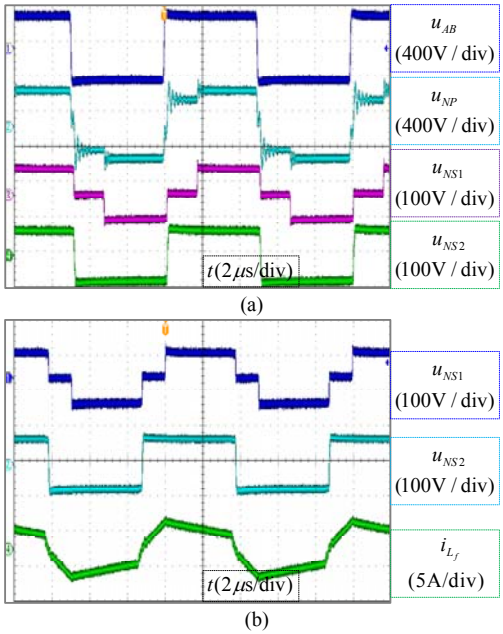

Fig. 14. Experimental waveforms at 80V and 1000W output, (a) waveforms of u_{AB} (voltage of middle-points of primary side bridge), u_{NP} (total voltage on primary winding s of the two transformers), u_{NS1} (voltage of secondary winding of T_1) and u_{NS2} (voltage of secondary winding of T_2), (b) u_{NS1}, u_{NS2} and i_{Lf} (current through the high-frequency-link inductor L_f).

Fig. 14 shows the waveforms of the DT-ADB converter with U_{in}=400V, U_o=80V and P_o=1kW. With the parameters, the converter works in CCM1 mode with voltage gain G>1. It can be seen from Fig. 14 that the switching waveforms meet the theoretical waveforms shown in Fig. 3 pretty well. The inductor current i_{Lf} decreases linearly during the main-power-transferring stage. The secondary winding voltage of the transformer T_2 is always clamped by the output voltage, which means it always transfers power to the load within the whole switching period. On the other hand, the secondary winding of transformer T_1 is shorted periodically to reset and charge the inductor current and control the power transmission from the input source to the load. Fig. 15 shows the waveforms when voltage gain G=1 (balance mode) and G<1 (buck mode). It can be seen that the inductor current keeps constant and declines linearly at the main-power-transferring stage, respectively.

Fig. 16 shows the waveforms when the converter works in the CCM2 and DCM mode, respectively. As shown in Fig. 16(a), when the converter works in the CCM2 mode, the inductor current increases linearly during the

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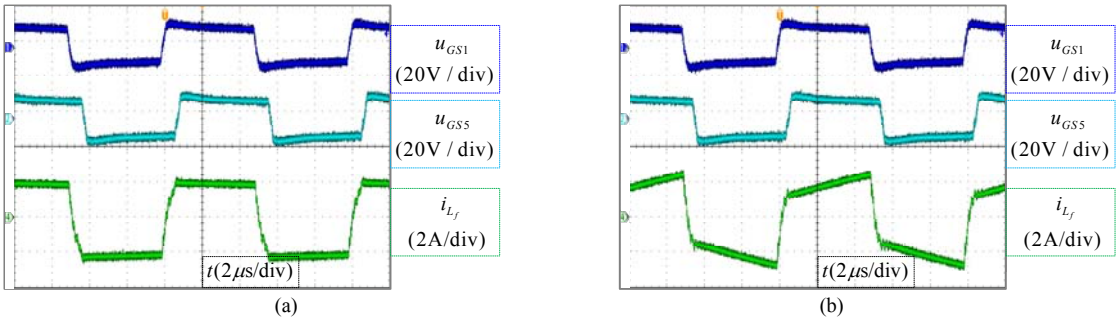

Fig. 15. Experimental waveforms of u_{GS1} (driving voltage of S_1), u_{GS5} (driving voltage of S_5) and i_{Lf}, (a) balance mode (b) buck mode.

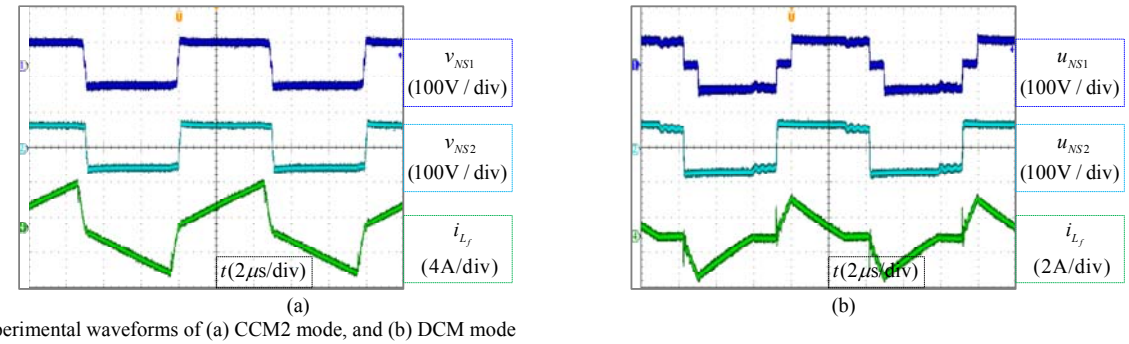

Fig. 16. Experimental waveforms of (a) CCM2 mode, and (b) DCM mode

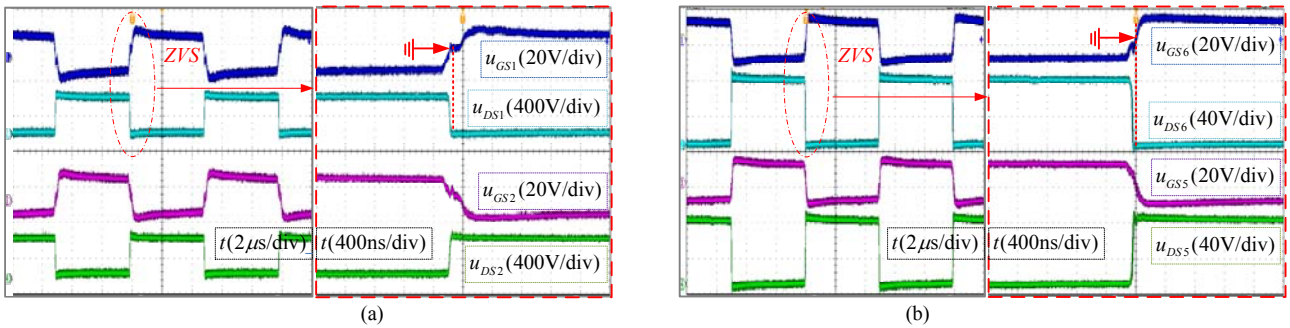

Fig. 17. Switching waveforms of (a) primary-side switches, (b) secondary-side switches.

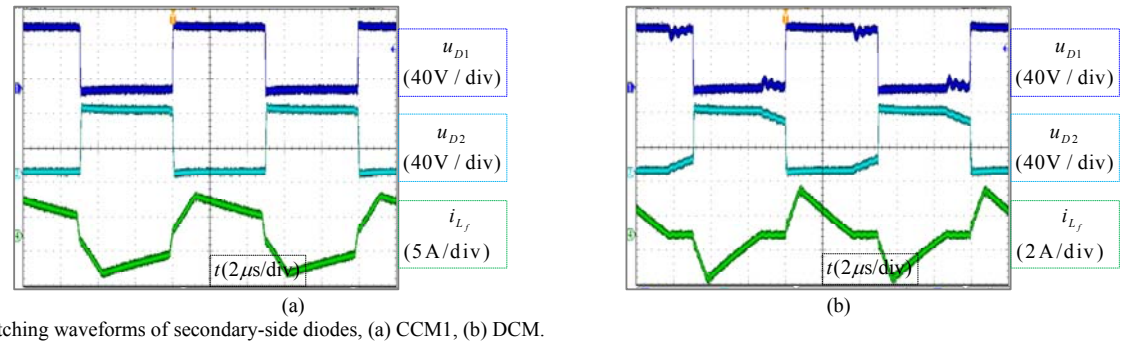

Fig. 18. Switching waveforms of secondary-side diodes, (a) CCM1, (b) DCM.

power-transferring-stage, which means the voltage gain G<1. When the converter works in the DCM mode, the current decreases during the power-transferring-stage with the voltage gain G>1.

The switching waveforms of the primary and secondary side switches are shown in Fig. 17. It can be seen that zero voltage switching (ZVS) is achieved for both the primary and secondary side switches. Since all the primary side switches work in the same pattern and both the secondary side switches work symmetrically, ZVS is accomplished for all the primary and secondary active switches. And there are no voltage spikes on the switches due to the soft switching.

The switching waveforms of the secondary-side diodes in the CCM1 and DCM are shown in Fig. 18(a) and (b), respectively, where u_{D1} and u_{D2} are the voltages on diode D_1 and D_2. It can be seen that the voltage stresses of the diodes are clamped to the output voltage without any voltage spikes or voltage ring. Furthermore, there is no reverse recovery

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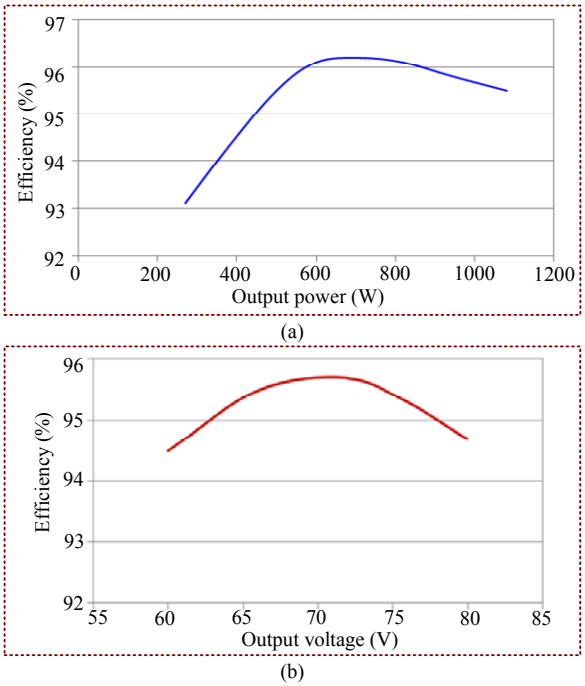

Fig. 19. Efficiency of the proposed DT-ADB converter, (a) at 72V output voltage, (b) at 1kW output power.

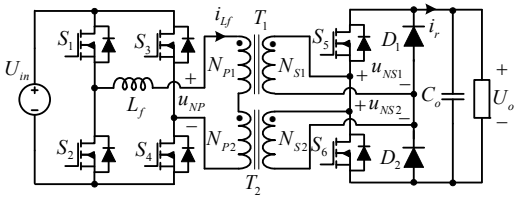

Fig. 20. Implementation of the compared prototype.

problem for the diodes because the current falling rate of the diode is controlled by the high-frequency-link inductor.

The efficiency curves versus output power under 72V output voltage is shown in Fig. 19(a). The peak efficiency is over 96%, and efficiency of 94% is achieved in a wide power range due to soft-switching operation, reduced inductor and distributed transformers. The efficiency curves versus output voltage under 1kW output power is shown in Fig. 19(b). It can be seen that high efficiency of over 94% is achieved within the whole output voltage range thanks to the wide voltage conversion gain and wide range of soft-switching of the proposed converter. And the peak efficiency is achieved when the converter works in the balance mode with voltage gain G=1. It is demonstrated that the converter is an excellent candidate for the wide voltage gain applications.

B. Comparison with Previous Converter

To show a fair comparison between the proposed converter and the previous converter, another experimental prototype using the topology presented in [20] is built based on the original prototype of the DT-ADB converter. The MOSFETs, diodes, high-frequency-link inductor and the transformers of the two prototypes are all the same. The two transformers in the DT-ADB converter are directly paralleled to implement the transformer in [20], as shown in Fig. 20. In this scenario, the two transformers, T_1 and T_2, are used as one transformer

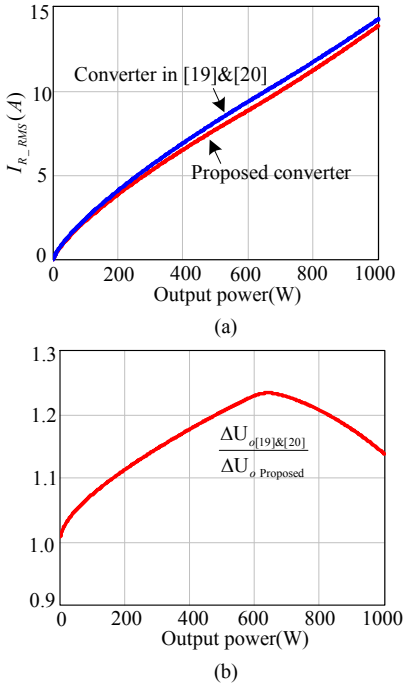

Fig. 21. Comparison of (a) root-mean-square value of rectified current, (b) voltage ripple of output capacitor.

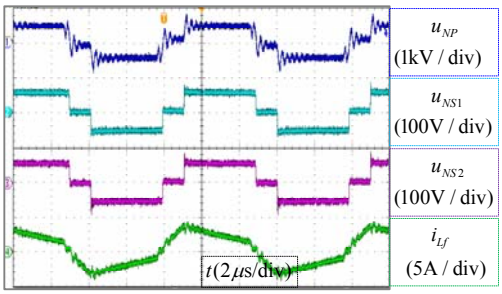

Fig. 22. Experimental waveforms of the compared converter.

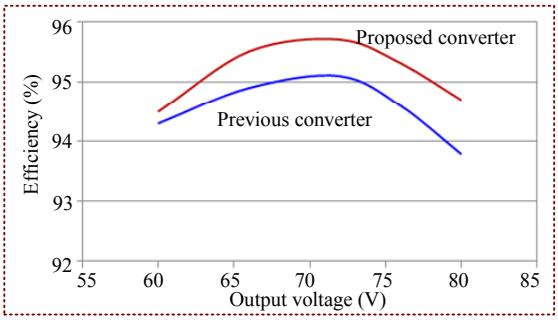

Fig. 23. Efficiency comparison of the proposed converter and previous converter at 1kW output power.

with equivalent turns ratio of 2N, and the normalized voltage gain of the previous converter and the DT-ADB converter is the same, which can make the comparison be fair.

Based on the specification given in Table II and when the output voltage is 80V, the root-mean-square value of rectified current i_r (before the output capacitor) and the voltage ripple on the output capacitor of both the proposed converter and the converters in [19] and [20] are calculated and shown in Fig. 21. It can be seen that, when the high-frequency-link inductor, the normalized voltage gain defined by (1), and the

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output capacitor are the same, the proposed converter can help to reduce the root-mean-square current of the output capacitances as well as output capacitance requirement for a given voltage ripple. Fig. 22 shows the experimental waveforms of this converter with U_{in}=400V, U_o=80V and P_o=1kW. The waveform of the inductor current i_{Lf} is nearly the similar to that of the DT-ADB converter, but the waveforms of the transformer windings of the two converters are different. Fig. 23 shows the measured efficiencies of the proposed converter and the compared converter. The tested results indicate that, when the high-frequency-link inductors and transformers are the same, higher conversion efficiency is achieved with the proposed converter.

V. Conclusion

In this paper, a secondary-side phase-shift-controlled soft-switching dual-transformer-based asymmetrical dual-bridge (DT-ADB) converter for high-efficiency, wide conversion range applications has been proposed and analyzed. The improved primary-side-series and secondary-side-parallel configuration halves the power and current rating of the two transformers, which help to reduce the transformer turns ratio, lower the power losses and thermal stresses of the magnetic components. Zero-voltage turn-ON of all the active switches and zero-current turn-OFF of all the diodes can be achieved to effectively reduce the switching losses. Furthermore, the current through the secondary side devices is effectively reduced, which largely reduces the turn-OFF losses of secondary side active switches and improves the efficiency of the converter. Moreover, the voltage applied on the high-frequency link inductor is effectively reduced, and hence the value and size of the inductor can be significantly reduced, which can help to improve the efficiency and power density. Continuous output current is also achieved when the converter operates in continuous current mode, which results in a smaller size of output filter. In addition, a wide conversion range can be achieved since the converter can work in three modes including the buck, balance, and boost modes. The analysis and performance have also been fully validated experimentally on a 100kHz, 1-kW hardware prototype.

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