Multi-Core Embedded Wireless Sensor Networks: Architecture and Applications

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Abstract—Technological advancements in the silicon industry, as predicted by Moore's law, have enabled integration of billions of transistors on a single chip. To exploit this high transistor density for high performance, embedded systems are undergoing a transition from single-core to multi-core. Although a majority of embedded wireless sensor networks (EWSNs) consist of single-core embedded sensor nodes, multi-core embedded sensor nodes are envisioned to burgeon in selected application domains that require complex in-network processing of the sensed data. In this paper, we propose an architecture for heterogeneous hierarchical multi-core embedded wireless sensor networks (MCEWSNs) as well as an architecture for multi-core embedded sensor nodes used in MCEWSNs. We elaborate several compute-intensive tasks performed by sensor networks and application domains that would especially benefit from multi-core embedded sensor nodes. This paper also investigates the feasibility of two multi-core architectural paradigms—symmetric multiprocessors (SMPs) and tiled many-core architectures (TMAs)—for MCEWSNs. We compare and analyze the performance of an SMP (an Intel-based SMP) and a TMA (Tilera's TILEPro64) based on a parallelized information fusion application for various performance metrics (e.g., runtime, speedup, efficiency, cost, and performance per watt). Results reveal that TMAs exploit data locality effectively and are more suitable for MCEWSN applications that require integer manipulation of sensor data, such as information fusion, and have little or no communication between the parallelized tasks. To demonstrate the practical relevance of MCEWSNs, this paper also discusses several state-of-the-art multi-core embedded sensor node prototypes developed in academia and industry. We further discuss research challenges and future research directions for MCEWSNs.

Index Terms—Wireless sensor networks, multi-core, embedded systems, symmetric multiprocessors, tiled many-core architecture, near-threshold computing, heterogeneous, compressive sensing

1 Introduction and Motivation

EMBEDDED wireless sensor networks (EWSNs) consist of sensor nodes with embedded sensors to sense data about a phenomenon and these sensor nodes communicate with neighboring sensor nodes over wireless links. Many emerging EWSN applications (e.g., surveillance, volcano monitoring) require a plethora of sensors (e.g., acoustic, seismic, temperature, and, more recently, image sensors and/or smart cameras) embedded in the sensor nodes. Although traditional EWSNs equipped with scalar sensors (e.g., temperature, humidity) transmit most of the sensed information to a sink node (base station node), this *sense-transmit* paradigm is becoming infeasible for information-hungry applications equipped with a plethora of sensors, including image sensors and/or smart cameras.

Processing and transmission of the large amount of sensed data in emerging applications exceeds the capabilities of traditional EWSNs. For example, consider a military EWSN deployed in a battlefield, which requires various sensors, such as imaging, acoustic, and electromagnetic sensors. This application presents various challenges for existing EWSNs since transmission of high-resolution images and video streams over bandwidth-limited wireless links from sensor nodes to the sink node is infeasible. Furthermore, meaningful processing of multimedia data (acoustic, image, and video in this example) in real-time exceeds the capabilities of traditional EWSNs consisting of single-core embedded sensor nodes [1], [2], and requires more powerful embedded sensor nodes to realize this application.

Since single-core EWSNs will soon be unable to meet the increasing requirements of information-rich applications (e.g., video sensor networks), next generation sensor nodes must possess enhanced computation and communication capabilities. For example, the transmission rate for the first generation Mica motes was 38.4 kbps whereas the second generation Mica motes (MicaZ motes) can communicate at 250 kbps using IEEE 802.15.4 (Zigbee) [3]. Despite these advances in communication, limited wireless bandwidth from sensor nodes to the sink node makes timely transmission of multimedia data to the sink node infeasible. In traditional EWSNs, the communication energy dominates the computation energy. For example, an embedded sensor node produced by Rockwell Automation [4] expends $2000\times$ more energy for transmitting a bit than that of executing a single instruction [5]. Similarly, transmitting a 15 frames per second (FPS) digital video stream over a wireless Bluetooth link takes 400 mW [6].

Fortunately, there exists a tradeoff between transmission and computation in an EWSN, which is well-suited for in-network processing for information-rich applications

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and allows transmission of only event descriptions (e.g., detection of a target of interest) to the sink node to conserve energy. Technological advancements in multi-core architectures have made multi-core processors a viable and cost-effective choice for increasing the computational ability of embedded sensor nodes. Multi-core embedded sensor nodes can extract the desired information from the sensed data and communicate only this processed information, which reduces the data transmission volume to the sink node. By replacing a large percentage of communication with in-network computation, multi-core embedded sensor nodes could realize large energy savings that would increase the sensor network's overall lifetime.

Multi-core embedded sensor nodes enable energy savings over traditional single-core embedded sensor nodes in two ways. First, reducing the energy expended in communication by performing *in-situ* computation of sensed data and transmitting only processed information. Second, a multi-core embedded sensor node allows the computations to be split across multiple cores while running each core at a lower processor voltage and frequency, as compared to a single-core system, which results in energy savings. Utilizing a single-core embedded sensor node for information processing in information-rich applications requires the sensor node to run at a high processor voltage and frequency to meet the application's delay requirements, which increases the power dissipation of the processor. A multi-core embedded sensor node reduces the number of memory accesses, clock speed, and instruction decoding, thereby enabling higher arithmetic performance at a lower power consumption as compared to a single-core processor [6].[1]

This paper investigates the feasibility of two multi-core architectures that can be used in processing units of embedded sensor nodes for multi-core embedded wireless sensor networks (MCEWSNs): symmetric multiprocessors (SMPs) and tiled many-core architectures (TMAs).[2] We consider SMPs because SMPs are ubiquitous and pervasive, which provides a standard/fair basis for comparing with other novel architectures (e.g., TMAs) [7]. We consider Tilera's TILEPro64 for TMAs because of Tilera's innovative architectural features (e.g., three-way issue superscalar tiles, on-chip mesh interconnect, and dynamic distributed cache (DDC) technology). Despite the diversity of application domains for MCEWSNs (e.g., military, health, satellites), many application domains have information fusion as one of the most critical applications, and hence we parallelize the information fusion application both for SMPs and TMAs. We compare and analyze the performance of an SMP (an Intel-based SMP) and a TMA (Tilera's TILEPro64) for performance evaluation.

The choice of a multi-core architecture dictates the high-level parallel languages since some multi-core architectures support proprietary parallel languages whose benchmarks are not available open source (e.g., Tilera's TILEPro64). Tilera provides a multi-core development environment (MDE) `ilib` API [8] whereas many SMPs (e.g., the Intel-based SMP) support OpenMP (Open Multi-processing), hence the *cross-architectural evaluation* results may be affected by the parallel language's efficiency. However, our analysis provides insights into the attainable performance per watt from these two multi-core architectures for MCEWSNs. To the best of our knowledge, this paper is the first to highlight the feasibility and application of multi-core technology in EWSNs. Although few initiatives study the feasibility of multi-core technology for EWSNs [9], [10], no prior work proposes an MCEWSN architecture based on multi-core embedded sensor nodes. Furthermore, motives and application domains for MCEWSNs have not yet been characterized. Our main contributions are as follows:

- Proposal of a heterogeneous hierarchical MCEWSN and associated multi-core embedded sensor node architecture.
- Elaboration on several computation-intensive tasks performed by sensor networks that would especially benefit from multi-core embedded sensor nodes.
- Characterization and discussion of various application domains for MCEWSNs.
- Discussion of several state-of-the-art multi-core embedded sensor node prototypes developed in academia and industry.[3]
- Parallelization of an information fusion application for two multi-core architectures (SMPs and TMAs) that can be used in embedded sensor nodes' processing units.
- Comparison and analysis of the performance and performance per watt of SMPs and TMAs based on our parallelized information fusion application. This analysis demonstrates performance and performance per watt advantages attained by multi-core embedded sensor nodes as compared to single-core embedded sensor nodes.

The remainder of this paper is organized as follows. Section 2 proposes an MCEWSN architecture. Potential application domains amenable to MCEWSNs are discussed in Section 3. Results are presented in Section 4. Section 5 discusses the research challenges and future research directions for MCEWNS and Section 6 concludes this paper.

2 Multi-Core Embedded Wireless Sensor Network Architecture

Fig. 1 depicts our proposed heterogeneous hierarchical MCEWSN architecture, which satisfies the increasing in-network computational requirements of emerging EWSN applications. The heterogeneity in the architecture subsumes the integration of numerous single-core embedded sensor nodes and several multi-core embedded sensor nodes. We note that homogeneous hierarchical single-core

1. The supplementary material which is available in the Computer Society Digital Library at http://doi.ieeecomputersociety.org/10.1109/219 document posted online discusses prior work related to multi-core embedded sensor nodes.

2. The discussion of sensor nodes' multi-core architectures and parallel computing metrics that we use to evaluate these architectures is presented in Section 3 of the supplementary material available online document.

3. Detailed in Section 5 of the supplementary material available online document.

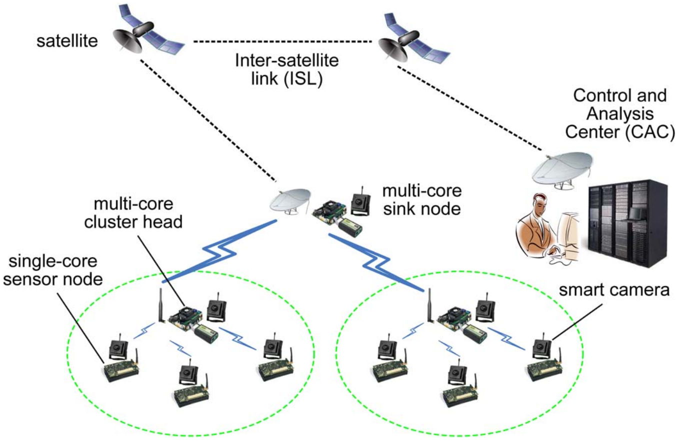

Fig. 1. A heterogeneous multi-core embedded wireless sensor network (MCEWSN) architecture.

EWSNs have been discussed in literature for large EWSNs (EWSNs consisting of a large number of sensor nodes) [11], [12]. Our proposed architecture is hierarchical since the architecture comprises of various clusters (a group of embedded sensor nodes in communication range with each other) and a sink node. A hierarchical network is well suited for large EWSNs since small EWSNs, which consist of only a few sensor nodes, can send the sensed data directly to the base station or sink node.

Each cluster consists of several leaf sensor nodes and a cluster head. Leaf sensor nodes contain a single-core processor and are responsible for sensing, pre-processing sensed data, and transmitting sensed data to the cluster head nodes. Since leaf sensor nodes are not intended to perform complex processing of sensed data in our proposed architecture, a single-core processor sufficiently meets the computational requirements of leaf sensor nodes. Cluster head nodes consist of a multi-core processor and are responsible for coalescing/fusing the data received from leaf sensor nodes for transmission to the sink node in an energy- and bandwidth-efficient manner. Our proposed architecture with multi-core cluster heads is based on practical reasons since sending all the collected data from the cluster heads to the sink node is not feasible for bandwidth limited EWSNs, which warrants complex processing and information fusion to be carried out at cluster head nodes and only the concise processed information is transmitted to the sink node.[4]

The sink node contains a multi-core processor and is responsible for transforming high-level user queries from the control and analysis center (CAC) to network-specific directives, querying the MCEWSN for the desired information, and returning the requested information to the user/CAC. The sink node's multi-core processor facilitates post-processing of the information received from multiple cluster heads. The post-processing at the sink node includes information fusion and event detection based on aggregated data from all of the sensor nodes in the network. The CAC further analyzes the information received from the sink node and issues control commands and queries to the sink node.

MCEWSNs can be coupled with a satellite backbone network that provides long-haul communication from the sink node to the CAC since MCEWSNs are often deployed in remote areas with no wireless infrastructure, such as a cellular network infrastructure. The satellites in the satellite backbone network communicate with each other via intersatellite links (ISLs). Since a satellite's uplink and downlink bandwidth is limited, a multi-core processor in the sink node is required to process, compress, and/or encrypt the information sent to the satellite backbone network.

Even though this paper focuses on heterogeneous MCEWSNs, homogenous MCEWSN architectures are an extension of our proposed architecture (Fig. 1) where leaf sensor nodes also contain a multi-core processor. In a homogeneous MCEWSN equipped with multiple sensors, each processor core in a multi-core embedded sensor node can be assigned to process one sensing task (e.g., one processor core handles sensed temperature data and another processor core handles sensed humidity data and so on) as opposed to single-core embedded sensor nodes where the single processor core is responsible for processing all of the sensed data from all of the sensors. We focus on heterogeneous MCEWSNs as we believe that heterogeneous MCEWSNs would serve as a first step towards integration of multi-core and sensor networking technology because of the following reason. Due to the dominance of single-core embedded sensor nodes in existing EWSNs, replacing all of the single-core embedded sensor nodes with multi-core embedded sensor nodes may not be feasible and cost-effective given that only a few multi-core embedded sensor nodes operating as cluster heads could meet an application's in-network computation requirements. Hence, our proposed heterogeneous MCEWSN would enable a smooth transition from single-core to multi-core EWSNs.[5]

3 MCEWSN Application Domains

MCEWSNs are suitable for sensor networking application domains that require complex in-network information processing such as wireless video sensor networks, wireless multimedia sensor networks, satellite-based wireless sensor networks, space shuttle sensor networks, aerial-terrestrial hybrid sensor networks, and fault-tolerant sensor networks. In this section, we discuss these application domains for MCEWSNs.[6]

3.1 Wireless Video Sensor Networks (WVSNs)

Wireless video sensor networks (WVSNs) are WSNs in which smart cameras and/or image sensors are embedded in the sensor nodes. WVSNs emulate the compound eye found in certain arthropods. Although WVSNs are a subset

4. Section 4 of the supplementary material available online document elaborates on several compute-intensive tasks that motivated the emergence of MCEWSNs.

5. Section 2 of the supplementary material available online document depicts the architecture of a multi-core embedded sensor node in our MCEWSN.

6. Section 5 of the supplementary material available online document describes several state-of-the-art multi-core embedded sensor node prototypes.

of wireless multimedia sensor networks (WMSNs), we discuss WVSNs separately to emphasize the WVSNs' stand-alone existence. WVSNs are suitable for applications in areas such as homeland security, battlefield monitoring, and mining. For example, video sensors deployed at airports, borders, and harbors provide a level of continuous and accurate monitoring and protection that is otherwise unattainable. We discuss the application of multi-core embedded sensor nodes both for image- and video-centric WVSNs.

In image-centric WVSNs, multiple image/camera sensors observe a scene from multiple directions and are able to describe objects in their true three-dimensional appearance by overcoming occlusion problems. Low-cost imaging sensors are readily available, such as CCD and CMOS imaging sensors from Kodak, and the Cyclops camera from the University of California at Los Angeles (UCLA) designed as an add-on for Mica sensor nodes [6]. Image preprocessing involves convolutions and data-dependent operations using a limited neighborhood of pixels. The signal processing algorithms for image processing in WVSNs typically exhibit a high degree of parallelism and are dominated by a few regular kernels (e.g., FFT) that are responsible for a large fraction of the execution time and energy consumption. Accelerating these kernels on multi-core embedded sensor nodes would achieve significant speedup in execution time and reduction in energy consumption, and would help achieve real-time computational requirements for many applications in energy-constrained domains.

Video-centric WVSNs rely on multiple video streams from multiple embedded sensor nodes. Since sensor nodes can only serve low-resolution video streams given the sensor nodes' resource limitations, a single video stream alone does not contain enough information for vision analysis such as event detection and tracking, however, multiple sensor nodes can capture video streams from different angles and distances together providing enormous visual data [3]. Video encoders rely on intraframe compression techniques that reduce redundancy within one frame and interframe compression techniques (e.g., predictive coding) that exploit redundancy among subsequent frames [1]. Video coding techniques require complex algorithms that exceed the computing power of single-core embedded sensor nodes. The visual data from numerous sensor nodes can be combined to give high-resolution video streams, however, this processing requires multi-core embedded sensor nodes and/or cluster heads.

3.2 Wireless Multimedia Sensor Networks (WMSNs)

A wireless multimedia sensor network (WMSN) consists of wirelessly connected embedded sensor nodes that can retrieve multimedia content such as video and audio streams, still images, and scalar sensor data of the observed phenomenon. WMSNs target a large variety of distributed, wireless, streaming multimedia networking applications ranging from home surveillance to military and space applications. A multimedia sensor captures audio and image/video streams using an embedded microphone and a micro-camera.

Various sensors in a WMSN coordinate closely to achieve application goals. For example, in a military application for target detection and tracking, acoustic and electromagnetic sensors can enable early detection of a target but may not provide adequate information about the target. Additional target details, such as type of vehicle, equipped armaments, and onboard personnel, are often required and gathering these details requires image sensors. Although the sensing ability in most sensors is isotropic and attenuates with distance, a distinct characteristic of video/image sensors is these sensors' directional sensing ranges. Recently, omnicameras have become available, which can provide complete coverage of the scene around a sensor node, however, applications are limited to close range scenarios to guarantee sufficient image resolution for moving objects [3]. To ensure full coverage of the sensor field, a set of directional cameras is required to capture enough information for activity detection. The image and video sensors high sensing cost limits these sensors continuous activation given constrained embedded sensor node resources. Hence, the image and video sensors in a WMSN require sophisticated control such that the image and video sensors are triggered only after a target is detected based on sensed data from other lower cost sensors, such as acoustic and electromagnetic.

Desirable WMSN characteristics include the ability to store, process in real-time, correlate, and fuse multimedia data originating from heterogeneous sources [1]. Multimedia contents, especially video streams, require data rates that are orders of magnitude higher than those supported by traditional single-core embedded sensor nodes. To process multimedia data in real-time and to reduce the wireless bandwidth demand, multi-core embedded sensor nodes in the network are required. Multi-core embedded sensor nodes facilitate *in-situ* processing of voluminous information from various sensors, notifying the CAC only once an event is detected (e.g., target detection).

3.3 Satellite-Based Wireless Sensor Networks (SBWSN)

A satellite-based wireless sensor network (SBWSN) is a wireless communication sensing network composed of many satellites, each equipped with multi-functional sensors, long-range wireless communication modules, thrusters for attitude adjustment, and a computational unit (potentially multi-core) to carry out processing of the sensed data. Traditional satellite missions are extremely expensive to design, build, launch, and operate, thereby motivating the aerospace industry to focus on distributed space missions, which would consist of multiple small, inexpensive, and distributed satellites coordinating to attain mission goals. SBWSNs would enable robust space missions by tolerating the failure of a single or a few satellites as compared to a large single satellite, where a single failure could compromise the success of a mission. SBWSNs can be used for a variety of missions, such as space weather monitoring, studying the impact of solar storms on Earth's magnetosphere and ionosphere, environmental monitoring (e.g., pollution, land, and ocean surface monitoring), and hazard prediction (e.g., flood and earthquake prediction).

Each SBWSN mission requires specific orbits and constellations to meet mission requirements and GPS provides an essential tool for orbit determination and navigation. Typical constellations include string-of-pearls, flower constellation, and satellite cluster. In particular, the flower constellation provides stable orbit configurations, which are suitable for *micro-satellite*(mass < 100 kg), *nano-satellite*(mass < 10 kg), and *pico-satellite*(mass < 1 kg) missions. Important orbital factors to consider in SBWSN design are relative range (distance) and speed between satellites, the inter-satellite link (ISL) access opportunity, and the ground-link access opportunity. The access time is the time for two satellites to communicate with each other and depends on the distance between the satellites (range). Satellites in an SBWSN can be used as an interferometer, which correlates different images acquired from slightly different angles/view points in order to get better resolution and more meaningful insights.

All of the satellites in an SBWSN collaborate to sense the desired phenomenon, communicate over long distances through beam-forming over an ISL, and maintain the network topology through self-organized mobility [13]. Studies indicate that IEEE 802.11b (Wi-Fi) and IEEE 802.16 (WiMax) can be used for inter-satellite communications (communication between satellites) and IEEE 802.15.4 (Zigbee) can be used for intra-satellite (communication between sensor nodes within a satellite) communications [14]. We point out that the IEEE 802.11b protocol requires modifications for use in an ISL where the distance between satellites is more than one kilometer since the IEEE 802.11b standard normally supports a communication range within 300 meters. The feasibility of wireless protocols for inter-satellite communication depends on the range, power requirements, medium access control (MAC) features, and support for mobility. The intra-satellite protocols are mainly selected based on power since the range is small within a satellite. A low duty cycle and the ability to put the radio to sleep are desirable features for intra-satellite communication protocols. For example, the MICA2DOT mote, which requires 24 mW of active power and 3 μW of standby power, supplied by a 3 V 750 mAh battery cell can last for 27,780 hours $\approx$ three years and two months, while operating at a duty cycle of 0.1 percent (supported by Zigbee) [15].

Since an individual satellite within an SBWSN may not have sufficient power to communicate with a ground station, a sink satellite in an SBWSN can communicate with a ground station, which is connected to the CAC. Ground communication in SBWSNs takes place in very-high frequency (VHF) (30 MHz-300 MHz) and ultra-high frequency (UHF) (300 MHz-3 GHz) bands. VHF frequencies pass through the ionosphere with effects, such as scintillation, fading, Faraday's rotation, and multi-path effects during intense solar cycles due to reflection of the VHF signals. UFH frequencies, in which both S- and L-bands lie, can suffer severe disruptions during a solar storm. For a formation of several SNAP-1 nano-satellites, the typical downlink data rate is 38.4 kbps or 76.8 kbps maximum [15], which necessitates multi-core embedded sensor nodes in SBWSNs to perform *in-situ* processing so that only event descriptions are sent to the CAC.

3.4 Space Shuttle Sensor Networks (3SN)

A space shuttle sensor network (3SN) corresponds to a network of sensors aimed to monitor a space shuttle during pre-flight, ascent, on-orbit, and re-entry phases. Battery-operated embedded wireless sensors can be easily bonded to the space shuttle's structure and enable real-time monitoring of temperature, triaxial vibration, strain, pressure, tilt, chemical, and ultrasound data. MCEWSNs would enable real-time monitoring of space vehicles not possible by ground-based sensing systems. For example, the Columbia space shuttle accident was caused by damage done when foam shielding dislodged from the external fuel tank during the shuttle's launch, which damaged the wing's leading edge panels [16]. The vehicle lacked on-board sensors that could have enabled ground personnel to determine the extent and location of the damage. Ground-based cameras captured images of the impact but were not able to reliably characterize the location and severity of the impact and resulting damage.

MCEWSNs for space shuttles, currently under development, would be used for space shuttle main engine (SSME) crack investigation, space shuttle environmental control life support system (ECLSS) oxygen and nitrogen flexhose analysis, and wing leading edge impact detection. Since the amount of data acquired during the 10-minute ascent period is nearly 100 MB, the time to download all data, even for a single event, via the radio frequency (RF) link is prohibitively long. Hence, information fusion algorithms are required in 3SNs to minimize the quantity and increase the quality of data being transmitted via the RF link. Furthermore, MCEWSNs would enable a 10$\times$ reduction in the installation costs for the shuttle as compared to the sensing systems based on traditional wired approaches [16].

3.5 Aerial-Terrestrial Hybrid Sensor Networks (ATHSNs)

Aerial-terrestrial hybrid sensor networks (ATHSNs), which consist of ground sensors and aerial sensors, integrate terrestrial sensor networks with aerial/space sensor networks. To connect remote terrestrial EWSNs to a CAC located far away in urban areas, ATHSNs can include a satellite backbone network. The satellite backbone network is widely available at remote locations and provides a reliable and broadband communication network [17], [18]. Various satellite communication choices are possible, such as WildBlue, HughesNet, and NASA's geostationary operational environmental satellite (GOES) system. However, a satellite's uplink and downlink bandwidth is limited, and requires pre-processing as well as compression of sensed data, especially multimedia data such as image and video streams. Multi-core embedded sensor nodes are suitable for ATHSNs, and are capable of carrying out the processing and compression of high-quality image and video streams for transmission to and from a satellite backbone network.

Aerial networks in ATHSNs may consist of unmanned aerial vehicles (UAVs) and satellites. For example, consider an ATHSN in which UAVs contain embedded image and video sensors such that only the image scenes that are of significant interest from a military strategy perspective are sensed in greater detail. The working of ATHSNs consisting of UAVs and satellites can be described concisely in seven steps [17]: 1) Ground sensors detect the presence of a hostile target in the monitored field and store events in memory; 2) The satellite periodically contacts multi-core cluster heads in the terrestrial EWSN to download updates about the target's presence; 3) Satellites contact UAVs to acquire image data about the scene where the intrusion is detected; 4) UAVs gather image data through the embedded image sensors; 5) The embedded multi-core sensors in UAVs process and compress the image data for transmission to the satellite backbone network in a bandwidth-efficient manner; 6) The satellite backbone network relays the processed information received from the UAVs to the CAC; 7) The satellite backbone network relays the commands (e.g., launching the UAVs' arsenals) from the CAC to the UAVs.

Ye *et al.* [18] have implemented an ATHSN prototype for an ecological study using temperature, humidity, photosynthetically active radiation (PAR), wind speed, and precipitation sensors. The prototype consists of a small satellite dish and a communication modem for integrating a terrestrial EWSN with the WildBlue satellite backbone network, which provides commercial service. The prototype uses Intel's Stargate processor as the sink node, which provides access control and manages the use of the satellite link.

The transformational satellite (TSAT) system is a future generation satellite system that is designed for military applications by National Aeronautics and Space Administration (NASA), the U.S. Department of Defense (DoD), and the Intelligence Community (IC) [17]. The TSAT system is a constellation of five satellites, placed in geostationary orbit, that constitute a high-bandwidth satellite backbone network, which allows terrestrial units to access optical and radar imagery from UAVs and satellites in real-time. TSAT provides broadband, reliable, worldwide, and secure transmission of data. TSAT supports RF communication links with data rates up to 45 Mbps and laser communication links with data rates up to 10-100 Gbps [17].

3.6 Fault-Tolerant (FT) Sensor Networks

The sensor nodes in an EWSN are typically deployed in harsh and unattended environments, which makes fault-tolerance (FT) an important consideration in EWSN design, particularly for space-based WSNs. For example, the temperature of aerospace vehicles varies from cryogenic to extremely high temperature, and pressure from vacuum to very high pressure. Additionally, shock and vibration levels during launch can cause component failures. Furthermore, high levels of ionizing radiation requires electronics to be FT if not radiation-hardened (rad-hard). Multi-core embedded sensors can provide hardware-based (e.g., triple modular redundancy (TMR) or self-checking pairs (SCP)) as well as software-based (e.g., algorithm-based fault tolerance (ABFT)) FT mechanisms for applications requiring high reliability. Computations, such as pre-processing and data fusion, can be replicated on multiple cores so that if radiation corrupts processing on one core, processing on other cores would still enable reliable computation of results.

4 Results

In this section, we present performance and performance per watt results for the two multi-core architectures (SMPs and TMAs) that can be used in MCEWSNs. For the SMP architecture, we evaluate an eight-core Intel-based SMP consisting of two Intel Xeon E5430 quad-core processors fabricated at 45 nm CMOS lithography [19] with a maximum clock frequency of 2.66 GHz [7]. For conciseness, we will refer to this SMP as $\mathrm{SMP}^{2\times\mathrm{QuadXeon}}$ in the remainder of this paper. Results in this paper focus only on parallelization to demonstrate the performance and performance per watt advantages that can be attained by leveraging multi-core embedded sensor nodes. Implementation of a complete MCEWSN architecture (Fig. 1) for real-world applications, such as video surveillance, is a focus of our future research work. Considering the significance of information fusion for EWSNs, we parallelize an information fusion application both for SMPs and TMAs to investigate the suitability of the two architectures for MCEWSNs. We analyze an information fusion application as an example to demonstrate the performance and performance per watt advantages of multi-core embedded sensor nodes as compared to single-core embedded sensor nodes, although other sensor applications can be parallelized to demonstrate similar advantages.[7]

We parallelize the information fusion application for SMPs and TMAs using OpenMP and Tilera's MDE `ilib` API. The purpose of this comparison between SMPs and TMAs is to investigate the feasibility of SMPs and TMAs as multi-core processor architectures for cluster heads and sink nodes in MCEWSNs. This comparison also reveals the advantages of using a multi-core processor over a single-core processor in embedded sensor nodes in terms of performance and performance per watt.

We obtain the power consumption values of the SMPs and TMAs from the devices' respective datasheets and use these values in our power model[8] [7]. For example, the TILEPro64 has maximum active and idle mode power consumptions of 28 W and 5 W, respectively [20], [21]. Intel's Xeon E5430 has a maximum power consumption of 80 W and a minimum power consumption of 16 W in an extended HALT state [19], [22].

$\mathrm{SMP}^{2\times\mathrm{QuadXeon}}$'s performance results for the information fusion application are depicted in Table 1, where $N = 3{,}000{,}000$ event-triggered samples and the moving average filter window size is $M = 40$. T_s and T_p denote the serial and parallel run times, respectively. MOPS denotes Mega operations per second and MOPS/W denotes MOPS per watt. In order to optimize the application to the architecture as much as possible, we used compiler optimization

7. Section 6 of the supplementary material available online document presents further details on our experimental setup.

8. Eq. (1) in the supplementary material available online document.

TABLE 1
Performance Results for the Information Fusion Application for $\mathrm{SMP}^{2\times\mathrm{QuadXeon}}$ When $M = 40$

Problem Size N	# of Cores p	Execution Time (s) T_p	Speedup $S = T_s/T_p$	Efficiency $E = S/p$	Cost $C = T_p \cdot p$	Perf. (MOPS)	Perf. per watt (MOPS/W)
3000,000	1	12.02	1	1	12.02	1073.2	22.36
3000,000	2	7.87	1.53	0.76	15.74	1639.14	25.61
3000,000	4	4.03	2.98	0.74	16.12	3201	33.34
3000,000	6	2.89	4.2	0.7	17.34	4463.67	34.87
3000,000	8	2.48	4.85	0.61	19.84	5201.6	32.51

level −O3. As an example, $\mathrm{SMP}^{2\times\mathrm{QuadXeon}}$ (an eight-core processor) reveals a 4.85× speedup in MOPS as compared to a single-core processor. Additionally, the performance per watt results reveal the multi-core system's power efficiency. As an example, a four-core ($p = 4$) SMP-based processor attains 49 percent better performance per watt as compared to a single-core processor. These results verify that SMP-based sensor nodes are more performance- and power-efficient as compared to single-core sensor nodes.

Table 2 depicts the performance results for the information fusion application, obtained with the compiler optimization level −O3, for the TMA-based multi-core processor (TILEPro64) when $N = 3{,}000{,}000$ and $M = 40$. Results reveal that the TMA-based multi-core processor speeds up the execution time proportionally to the number of tiles p (i.e., ideal speed up) as compared to a comparable single-core processor (i.e., executing the application on a single TMA tile). The efficiency remains close to one and the cost remains nearly constant as the number of tiles increases indicating ideal scalability of the TMA-based multi-core processor for the information fusion application. For example, the TMA-based multi-core processor increases MOPS and MOPS/W by 48.4× and 11.3×, respectively, for $p = 50$ as compared to a single TMA tile.

These results verify that TMAs provide better performance per watt as compared to a comparable single processor-core architecture. Hence, an embedded sensor node using TMAs as processing units is more performance- and power-efficient as compared to an embedded sensor node using a single-core processing unit.

Fig. 2 compares the $\mathrm{SMP}^{2\times\mathrm{QuadXeon}}$ and the TILEPro64 with respect to performance per watt for a varying number of cores/tiles for the information fusion application. As an example, for an eight-core/tile system, the TILEPro64's performance per watt is 466 percent higher than the SMP's performance per watt. In summary, results show that the TILEPro64 provides improved performance per watt as compared to the $\mathrm{SMP}^{2\times\mathrm{QuadXeon}}$ mainly due to the fact that the information fusion application operates on private data that can be parallelized using the `ilib` API. This parallelization exploits high data locality when operating on the sensed data, which enables fast access to private data and results in higher internal memory bandwidth, and thus increased MOPS and MOPS/W.

There are two main reasons why the $\mathrm{SMP}^{2\times\mathrm{QuadXeon}}$ attains lower performance than the TILEPro64 for information fusion. First, shared memory applications are more suited to SMP architectures, which can exploit data locality more effectively. Second, the OpenMP-based parallel programming constructs `sections` and `parallel` forces operating threads to share data even if the data can be independently processed by each thread. When we parallelized the information fusion application for the $\mathrm{SMP}^{2\times\mathrm{QuadXeon}}$, we first tried using independent copies of the data for each thread, similarly to the TILEPro64, however, this introduced large memory requirements and subsequently segmentation faults. Therefore, we were forced to store the data in shared memory since OpenMP currently does not support specifying private data for individual threads, even though private data can be indicated for all the parallel computation threads. Consequently, inherent OpenMP limitations that preclude the declaration of thread-specific private data partially accounts for the SMP's lower performance. On the contrary,

TABLE 2
Performance Results for the Information Fusion Application for the TILEPro64 When $M = 40$

Problem Size N	# of Tiles p	Execution Time (s) T_p	Speedup $S = T_s/T_p$	Efficiency $E = S/p$	Cost $C = T_p \cdot p$	Perf. (MOPS)	Perf. per watt (MOPS/W)
3000,000	1	70.65	1	1	70.65	182.6	34.07
3000,000	2	35.05	2	1	70.1	368	64.33
3000,000	4	17.18	4.1	1.02	68.72	750.87	116.6
3000,000	6	11.48	6.2	1.03	68.9	1123.69	156.94
3000,000	8	8.9	7.94	0.99	71.2	1449.44	183.94
3000,000	10	6.79	10.4	1.04	67.9	1899.85	221.17
3000,000	50	1.46	48.4	0.97	73	8835.62	384.66

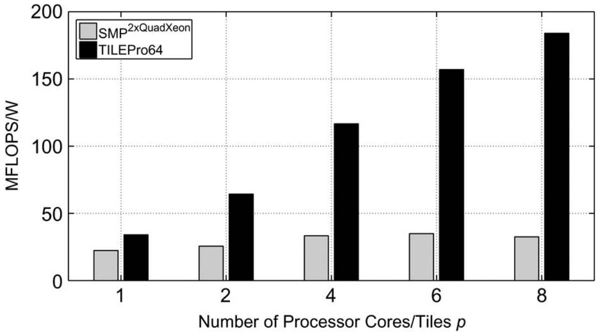

Fig. 2. Performance per watt (MOPS/W) comparison between $\mathrm{SMP}^{2\times \mathrm{QuadXeon}}$ and the TILEPro64 for the information fusion application when $N = 3{,}000{,}000$.

Tilera's ilib API permits ideal data distribution for the information fusion application (i.e., data that is received from the first source is only private to the first thread, and the other threads have no information on this data, data that is received from the second source is only private to the second thread, and so forth).

5 Research Challenges and Future Research Directions

Despite few initiatives towards MCEWSNs, the domain is still in its infancy and requires addressing some challenges to facilitate ubiquitous deployment of MCEWSNs. In this section, we discuss several research challenges and future research directions for MCEWSNs.

5.1 Application Parallelization

Parallelization of existing serial applications and algorithms can be challenging considering the limited number of parallel programmers as compared to serial programmers. Parallel applications with limited scalability present challenges for efficient utilization of multi-core and future many-core embedded sensor nodes. Furthermore, synchronization between different cores by the use of barriers and locks limit the attainable speedup from parallel applications. A poor speedup due to limited scalability as the number of cores increases can diminish the energy and performance benefits attained by parallelization of sensor applications. To minimize potential performance degradation for parallel applications with limited scalability, designers can restrict these applications to a limited number of cores while turning off remaining cores to save power or utilizing other cores by multiprogramming other sensor applications on those cores. Consequently, existing operating systems for embedded sensor nodes (e.g., TinyOS [23], MANTIS [24]) would require updating their schedulers for efficient scheduling of multi-programmed workloads and would also require some middleware support (e.g., OpenMP) to support multi-threading of parallel applications.

5.2 Signal Processing & Computer-Vision

Advances in sensor technology have led to a dramatic increase in the amount of data sensed, which is fueled by both the reduced cost of sensors and increased deployment over a large class of applications. This sensed data deluge problem exacerbates for MCEWSNs and places immense stress on our ability to process, store, and obtain meaningful information from the data. The fundamental reason behind the data deluge problem comes from sensor designs that are based on the Nyquist sampling theorem [25], which has been the dogma in traditional signal processing. However, as we build sensors and sensing platforms with increasing capabilities (e.g., MCEWSNs involving hyperspectral imaging), designs based on Nyquist sampling are prohibitively costly because of high-resolution sensors and extremely fast data processing requirements. The failure of Nyquist sampling lies in its inability to exploit redundant structures in signals. This redundancy and compressibility in signals forms the basis of Fourier and wavelet transforms. Research in sensing and processing systems that exploit the redundant structures in signals include sparse models, union-of-subspace models, and low-dimensional manifold models. The data deluge problem in MCEWSNs can be addressed in three fundamental ways: 1) parsimonious signal representations that facilitate efficient processing of visual signals; 2) novel compressive and computational imaging systems for sensing of data; and 3) scalable algorithms for large scale machine learning systems. These novel techniques to address the data deluge problem in MCEWSNs requires further research.

Another related research avenue for MCEWSNs is compressive sensing for high-dimensional visual signals, which requires sensors with capabilities that go beyond sensing two-dimensional (2D) images. Examples of these novel sensors include the Lytro camera for sensing light fields [26], the Kinect system that provides scene depth [27], and flexible camera-arrays that provide unique tradeoffs in the spatial, temporal, and angular resolutions of the incident light. Design of novel models, sensors, and technologies is imperative to better characterize objects with complex visual properties.

Furthermore, distilling information from a large number of low-resolution video streams obtained from multiple video sensors requires novel algorithms since current computer-vision and signal processing algorithms can only analyze a few high-resolution images.

5.3 Reconfigurability

Reconfigurability in MCEWSNs is an important research avenue that would allow the network to adapt to new requirements by integrating code upgrades (e.g., a more efficient algorithm for video compression may be discovered after deployment). Mobility and self-adaptability of embedded sensor nodes requires further research to obtain the desired view of the sensor field (e.g., an image sensor facing downward towards the earth may not be desirable).

5.4 Energy Harvesting

Considering that the battery energy is the most critical resource constraint for sensor nodes in MCEWSNs, research and development in energy-efficient batteries and energy-harvesting systems would be beneficial for MCEWSNs.

5.5 Near-Threshold Computing (NTC)

NTC refers to using a supply voltage (V_{DD}) that is close to a single transistor's threshold voltage V_t (generally V_{DD} is slightly above V_t in near-threshold operation whereas V_{DD} is below V_t for sub-threshold operation). Lowering the supply voltage reduces power consumption and increases energy efficiency by lowering the energy consumed per operation. With the advent of MCEWSNs leveraging many-core chips, sub- or near-threshold designs become a natural fit for these highly parallel architectures. Considering the stringent power constraints of the many-core chips leveraged in MCEWSNs, sub- or near-threshold designs may be the only practical way to power up all of the cores in these chips [28]. Hence, NTC provides a promising solution for the *dark silicon* problem (transistor under-utilization) in many-core architectures. However, widespread adoption of NTC in MCEWSNs for reduced power consumption requires addressing NTC challenges such as increased process, voltage, and temperature variations, subthreshold leakage power, and soft error rates.

5.6 Heterogeneous Architectures

MCEWSNs would benefit from parallel computer architecture research. Specifically, a heterogeneous many-core architecture that could leverage both super- and near-threshold computing to meet performance and energy requirements of sensing applications might provide a promising solution for MCEWSNs. The heterogeneous architecture can integrate super-threshold (nominal voltage) SMP cores and near-threshold single instruction multiple data (SIMD) cores [29]. Research indicates that a combination of NTC and parallel SIMD computations achieves excellent energy efficiency for easy-to-parallelize applications [30]. With this heterogeneous architecture, sensing applications' tasks with less parallelism can be scheduled to high-power SMP cores whereas tasks with abundant parallelism will benefit from scheduling on low-power near-threshold SIMD cores. Hence, research in heterogeneous architectures would enable a single architecture to serve a broad range of sensing applications with varying degrees of parallelism.

5.7 Transistor Technology

With ongoing technology scaling, conventional planar CMOS devices suffer from increasing susceptibility to numerous variations, such as circuit performance, short channel effects, delay, or leakage. Research in novel transistor technologies that improve the energy efficiency, provide better resistance to process variation, and are amenable for nano-scale fabrication would benefit sensor nodes in MCEWSNs. One of the promising transistor technologies for future process nodes (22 nm and below) is FinFET, in which the channel is a slab (fin) of undoped silicon perpendicular to the substrate [31]. The increased electrostatic control of the FinFET gate over the channel enables high on-current to off-current ratio, which improves carrier mobility, and is promising for near-threshold low-power designs. Other advantages of FinFET over planar CMOS include reduced random dopant fluctuations, lower parasitic junction capacitance, suppression of short channel effects, leakage currents, and parametric variations. However, the widespread transition to FinFET requires further research in prediction models for performance, energy, and process variation for this transistor technology as well as a complete overhaul of the current fabrication process.

6 Conclusion

In this paper, we proposed an architecture for heterogeneous hierarchical multi-core embedded wireless sensor networks (MCEWSNs). Compute-intensive tasks such as information fusion, encryption, network coding, and software defined radio, will benefit in particular from the increased computational power offered by multi-core embedded sensor nodes. Many wireless sensor networking application domains, such as wireless video sensor networks, wireless multimedia sensor networks, satellite-based sensor networks, space shuttle sensor networks, aerial-terrestrial hybrid sensor networks, and fault-tolerant sensor networks, can benefit from MCEWSNs. Perceiving the potential benefits of MCEWSNs, several initiatives have been undertaken in both academia and industry to develop multi-core embedded sensor nodes, such as InstraNode, satellite-based sensor nodes, and smart camera motes.

This paper evaluated two multi-core architectures, symmetric multiprocessors (SMPs) and tiled many-core architectures (TMAs), for multi-core embedded sensor nodes in an MCEWSN based on a parallelized information fusion application. Results revealed that the TILEPro64 exhibited better scalability and attained better performance per watt than the SMPs for the information fusion application. We further highlighted the research challenges and future research avenues for MCEWSNs. Specifically, MCEWSNs would benefit from advancements in application parallelization, signal processing, computer-vision, reconfigurability, energy harvesting, near-threshold computing, heterogeneous architectures, and transistor technology.

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