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Design of Reconfigurable Digital IF Filter with Low Complexity

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***Abstract*— Due to limited frequency resources, new services are being applied to the existing frequencies, and service providers are allocating some of the existing frequencies for newly enhanced mobile communications. Because of this frequency environment, repeater and base station systems for mobile communications are becoming more complicated, and frequency interference caused by multiple bands and services is getting worse. Therefore, a heterodyne receiver using IF filters with high selectivity has been used to minimize the interference between frequencies. However, repeater and base station systems in mobile communications employing fixed IF filters cannot actively cope with the usage of multiple frequency bands, the application of various services, and frequency recycling. Therefore, this brief proposes a reconfigurable digital IF filter with variable center frequency and bandwidth while achieving high selectivity as existing IF filters. The center frequency of filter can vary from 10MHz to 62.5MHz, and the filter bandwidth can be selective to one of 10MHz, 15MHz, and 20MHz. The proposed digital filter also reduces the complexity of adders and multipliers by 38.81% and 41.57%, respectively, compared to an existing digital filter by using a filter bank and a multi stage structure. This digital IF filter is fabricated on a 130-nm CMOS process and occupies 5.90 mm^2.**

***Index Terms*—digital filter, heterodyne system, intermediate frequency (IF), filter bank, multi-stage filter**

I. Introduction

RESENTLY, mobile communications has to ensure a wide frequency band to transmit a large amount of data with a high data rate. It is evolving into advanced communications such as LTE (4G services) to realize large amounts of data and fast transmission speed, and now has 5G mobile communications in the spotlight [1]. Therefore, spectrum allocation for mobile communications is becoming increasingly complicated. In base stations and repeaters, spectrum efficiency is maximized by using filters to minimize the interference of adjacent frequencies. The filters are employed to suppress crosstalk between adjacent signals, to minimize interference between transmission and reception frequencies, and to suppress spurious emissions caused by intermodulation in the system.

General base stations and repeaters in mobile communications adopt super-heterodyne receivers, which eliminate adjacent bands at intermediate frequency (IF) [2], [3]. This system generally utilizes analogue IF bandpass filters to minimize various frequency interference between heterogeneous services, adjacent service providers, and transmission and reception. These analog filters include an LC filter and a surface acoustic wave (SAW) IF filter. Recently, SAW filters have been replaced with digital IF filters based on finite impulse response (FIR) [4]. The SAW filter has high frequency stability and selectivity. However, when repeaters and base stations want to change the center frequency and bandwidth for new service adaptation, a new SAW filter should be developed and embedded due to its fixed frequency characteristics. As a result, system development is needed for the changed frequency environment or is supposed to adopt multiple SAW filters of two or more types, which causes both the increase of system costs and the delay in service opening. For these reasons, development of a variable digital filter responding to changeable frequency environments is required.

Variable digital FIR filters have been researched to be applied to various specifications of application services [5], [6]. Therefore, in this brief, we propose a reconfigurable digital IF filter that can adjust both the center frequency and bandwidth while maintaining high frequency selectivity as an existing fixed SAW filter. Since the digital bandpass filter of IF band needs to support high sampling rate, a large number of taps are required for high frequency selectivity, which results in increasing hardware complexity significantly. Various digital FIR structures with low complexity have been proposed in [7]. According to this tendency, in this brief, we propose a filter bank lowering the sampling rate in order to reduce the hardware complexity of a single digital bandpass filter. In addition, we also propose a bandpass filter with a recursive multi-stage structure working at a lower sampling rate.

II. Digital IF Filter System

A digital FIR filter can change its center frequency and bandwidth by adjusting filter coefficients. In this brief, we design a digital IF filter that sets coefficients from a software to change both the center frequency and the bandwidth. Since the hardware structure is likely to be fixed and has less flexibility,

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TABLE I
SPECIFICATION OF IF FILTER (3GPP [8], [9])

Item	Unit	MIN	TYP	MAX
Center frequency	MHz	-	62.5	-
Bandwidth	MHz	9.015		18.44
40 dB Bandwidth	MHz	11.6		21.6
Ultimate Rejection	dBc	40		
Insertion Loss	dB			10
ACRR[a]	dBc		20	
EVM[b]	%			8

[a]Adjacent channel rejection ratio
[b]Error vector magnitude

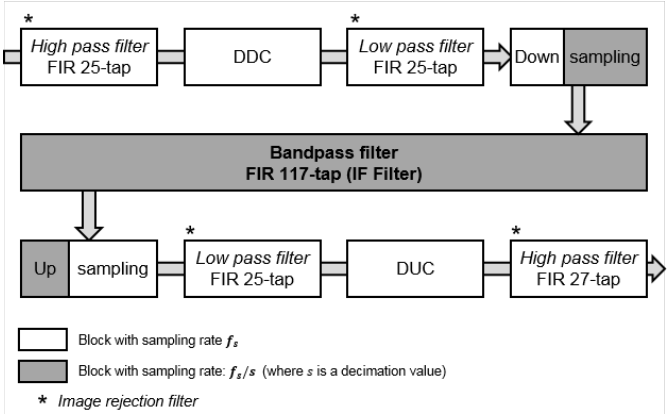

Fig. 1. Digital IF filter using Filter bank

the maximum number of taps has to be determined first. The maximum number of taps can be given from the required frequency response of filter, which is a function of a sampling rate, transition width (frequency gap between the end of pass band and the start of stop band), ripple in the pass band, and suppression in the stop band. In this brief, we design a filter depending on the specification of Table I according to the ITU standards [8] required for 3G and 4G mobile communication systems. The maximum number of taps needed in the filter can be obtained by using the MATLAB Filter Design & Analysis (FDA) tool. Since the required number of taps increases in proportion to the sampling rate, the maximum number of taps is given at the highest center frequency of IF band.

The digital IF filter requires a large number of taps, because the filter has to meet the specifications in Table 1 while working at a high sampling rate for high frequency selectivity. This causes the hardware resources of filter more complex. Therefore, in order to reduce the hardware complexity of filter, we propose both a filter bank structure using a digital down-converter (DDC) and a digital up-converter (DUC) and a bandpass filter structure using a multi-stage scheme.

A. Filter bank with a DDC and a DUC

In order to reduce the hardware complexity of digital IF filter, simple approach is to decrease sampling rate, which makes a filter bank structure adopt a DDC and a DUC. Since the number of taps highly depends on the sampling rate, to have the sampling rate lower at the same bandwidth is to reduce the complexity of filter effectively. The filter bank consists of a DDC, decimation (down sampling), interpolation (up sampling), and a DUC. It includes four image rejection filters (IRFs) to reject images that occur during down-conversion or up-conversion. As shown in Fig. 1, prior to the bandpass FIR filter, there are the DDC to lower the center frequency and decimation to reduce sampling rate, f_s. As the sampling rate is lowered due to the decimation process, f_s/s, the same filter performance can be achieved with fewer taps than an existing single digital filter. After bandpass filtering, up sampling is performed to recover the sampling rate, f_s, and the center frequency is moved to the original position through the DUC. Four IRFs with a few taps have to be deployed both before and after the DDC and DUC to remove images.

For the same frequency response of filter, the number of taps (N) can be decreased to N/s by reducing the sampling rate to $1/s$ in decimation. Because of digitized down-converting, however, the decimation value, s, in the proposed system has to have a natural value and be limited by several system parameters such as IF carrier frequency and bandwidth in commercial repeaters. A digital IF filter has to works in the given IF carrier frequency (from 10MHz to 65MHz), which has been generally used for

TABLE II
COMPARISON OF SINGLE DIGITAL FILTER AND PROPOSED DIGITAL FILTER USING FILTER BANK

SINGLE FILTER			FILTER USING FILTER BANK			
Tap	Multiplier	Adder	Tap	Multiplier	Adder	
			25	13	24	HPF
			25	13	24	LPF
			117	59	116	BPF
			25	13	24	LPF
			27	14	26	HPF
268	**134**	**267**	**219**	**112**	**214**	
Rate (%)			**18.28**	**16.42**	**19.85**	

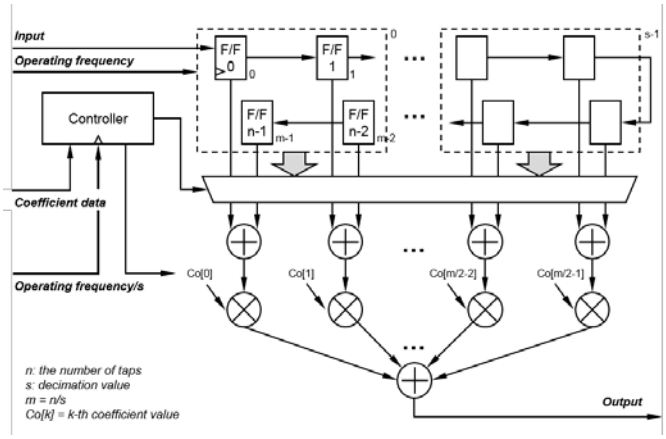

Fig. 2. Digital bandpass filter with Multi stage in Filter bank

TABLE III
COMPARISON OF SINGLE DIGITAL FILTER AND PROPOSED DIGITAL FILTER WITH MULTI STAGE

SINGLE FILTER			FILTER WITH MULTI STAGE			
Tap	Multiplier	Adder	Tap	Multiplier	Adder	
			25	13	24	HPF
			25	13	24	LPF
			117	**29**	**58**	**BPF**
			25	13	24	LPF
			27	14	26	HPF
268	**134**	**267**	219	**82**	**156**	
Rate (%)			-	**38.81**	**41.57**	

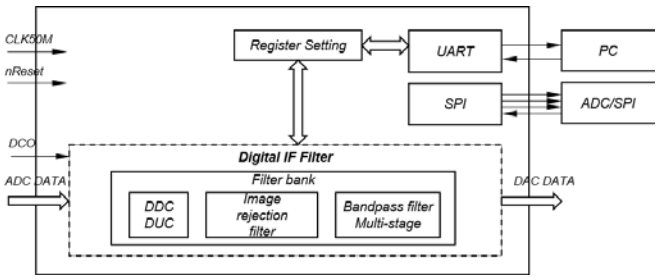

Fig. 3. Block diagram of digital IF filter.

analog IF SAW filters in commercial repeaters. For the given sampling rate and bandwidth, *s* is obtained, and then the optimized BPF can be designed for specifications required in the standard. For each IRF, the minimum number of taps is estimated in MATLAB simulation in order only to reject images. Since the filtered data of BPF is not corrupted through the image rejection process and the desired data are far away from images, the required number of taps for IRFs in the filter bank is very small as shown in Fig. 1. The low cost paid for IRFs makes the total number of taps effectively reduced. In this approach, the complexity of proposed filter can be reduced considerably.

We use the MATLAB FDA tool to generate the coefficient of filters in the proposed filter bank for the specifications given in Table I. As shown in Table II, the complexity of proposed filter using a filter bank can be reduced by 16.42% and 19.85% with respect to the number of multipliers and the adders, respectively, compared with the single digital filter without a filter bank.

B. Digital IF bandpass filter with multi-stage structure

In the bandpass filter in Fig. 1, which is a digital FIR filter working at the down sampling rate, it is possible to perform parallel operation when maintaining the original clock speed even after decimation process. Fig. 2 shows a block diagram of the proposed multi-stage structure. In the proposed multi-stage structure, the original structure of FIR filter is divided into *s* same structures by the ratio of decimation, *s*. The original *n*-order FIR filter requires *n-1* adders and *n/2*. When the data stream is decimated by the ratio of *s*, the speed of data fed into the filter is also reduced to *one-s*-th. The regular filter unit with *1/s* adders and *1/s* multipliers can perform the same work as the original *n*-order FIR filter by repeating filter operation *s* times recursively at the original working speed. With this approach, both the number of adders and multipliers can be reduced by *1/s* compared to an existing bandpass FIR filter without a multi-stage structure.

Table III compares the number of multipliers and adders of an existing single IF filter and the proposed IF filter using both the filter bank and the multi-stage structure. When *s* is 2, the hardware costs of multipliers and adders are reduced by 38.81% and 41.57%, respectively. The reduction ratio of proposed IF filter is higher in terms of hardware costs when the multi-stage structure is employed compared to the filter bank structure.

III. IMPLEMENTATION

Fig. 3 shows the system configuration of proposed digital IF filter. The proposed digital IF filter uses 3.3V I/O interface and 1.2V core voltage. It supports up to 200MHz operating frequency and includes a universal asynchronous receiver transmitter (UART) and a serial peripheral interface (SPI) with 50MHz operating frequency. The digital input and output have 12-bit and 14-bit resolutions, respectively. The filter coefficients for adjusting the center frequency and the bandwidth of IF filter is set via the UART from external control devices such as a micro-controller. In addition, the rate of DDC/DUC and down sampling rate used in the filter bank can be also controlled by the software.

TABLE IV
EXAMPLE OF PROPOSED DIGITAL IF FILTER

	Case 1	Case 2	Case 3
Center frequency (MHz)	62.6	42.5	10.0
Bandwidth (MHz)	20	20	10
DDC[a]	4:1	6:1	6:1
Down sampling[b]	2:1	2:1	2:1
Sampling rate (MHz)	165	144	144

[a]Sampling rate : Carrier frequency.
[b]Sampling rate : Down sampling rate.

TABLE V
CHIP SUMMARY

CMOS	130 nm
Work voltage	1.2 V/3.3 V
Gate count	386 K
Die size	2.43 mm × 2.43 mm
Operating Frequency	200 MHz
Power Consumption	408 mW

For reconfigurable filter implementation, the coefficients satisfying the filter specifications needed in mobile communications are pre-obtained by using the MATLAB FDA tool and can be also easily modified by only replacing the software. In this brief, in order to verify the re-configurability, we design the digital filters, which satisfy three types of frequency characteristics with different center frequencies and bandwidths, but the changeable specifications are not limited. For the test, we set the bandwidth of each filter, the ratio of the sampling frequency and the target frequency in the DDC/DUC, and the down/up sampling ratio in proportion to the original sampling rate as shown in Table IV.

A. Implementation on the CMOS technology and a test board

As shown in Table V and Fig. 4, the chip of digital IF filter is implemented on the 0.13μm CMOS process, and the die size of chip is 5.90mm^2. In order to verify the characteristics of the digital IF filter chip, a test board is also designed as shown in Fig. 5. The test board has 5V of an input voltage and includes a regulator for 3.3V, 1.2V, and 1.8V of supply powers for the designed digital chip. The digital IF filter test board can also be connected to the evaluation boards of a 12-bit resolution analog to digital converter (ADC: AD9627) and a 14-bit resolution digital to analog converter (DAC: AD9755). It contains level shifters to match I/O voltage between the ADC evaluation board and the designed digital chip and has various communication channels such as UART and universal serial bus (USB) for external PC.

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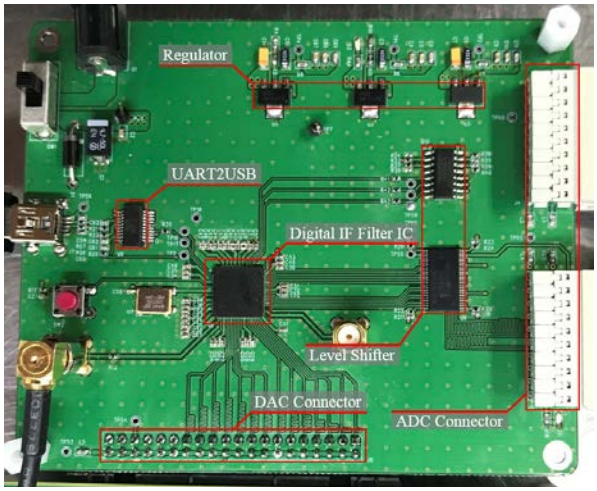


Fig. 4. Test board of proposed digital IF filter.

The test environments consist of a control PC that can set the system parameters of target digital IF filter such as the filter coefficients, a network analyzer to evaluate the required frequency characteristics of filter, and a spectrum analyzer to check for the filter satisfying the requirement of 3GPP standard.

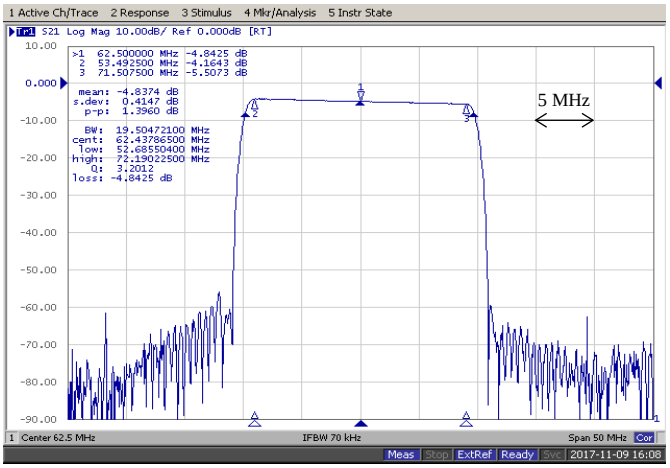
B. Measurements

Fig. 6 shows three types of frequency responses implemented on the reconfigurable digital IF filter: one with 62.5MHz of the center frequency and 20MHz of the bandwidth, another with 42.5MHz of the center frequency and 20MHz of the bandwidth, and the other with 10MHz of the center frequency and 10MHz of the bandwidth.

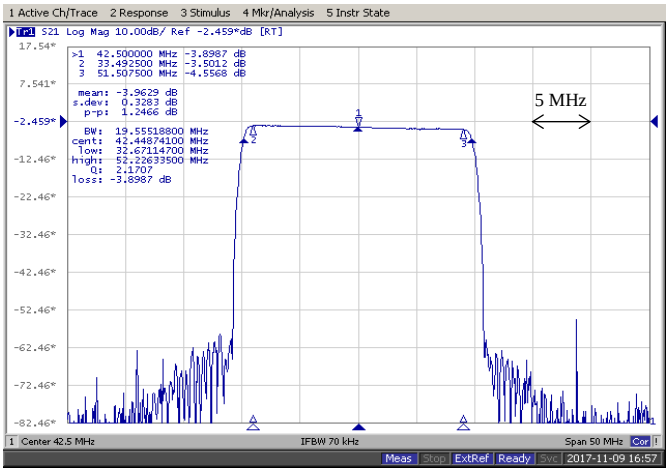
Table VI summarizes measurement results of the three types of filters implemented on the proposed reconfigurable IF filter. The bandwidth at the point of 40dB-loss is measured to 21.57MHz, 21.39MHz, and 11.29MHz, respectively, and the center frequencies are also measured as 62.43MHz, 42.45MHz, and 10.01MHz, respectively. The bandwidth at the point of 3dB-loss is measured to 19.35MHz, 19.67MHz, and 9.82MHz, respectively, which satisfy the required specifications. The insertion loss is also measured as -4.90dB, -3.56dB, and -2.79dB, respectively, and the ripple is measured as 1.36dB, 0.89dB and 0.48dB, respectively. The proposed filter has the absolute delay as 1.55μsec, 1.45μsec, and 1.78μsec, respectively. Commercial IF SAW filters [10], [11] have about 1-3μsec of absolute delay, and the requirement of time delay for the IF-filtering process in the standard [12] is about 5-6μsec. Therefore, the measured absolute delay (about 1.5-1.8μsec) of proposed filter is within both the commercial and the standard requirements. The EVM and the ACRR are tested when using a WCDMA signal through a signal generator. The measured EVM values are 1.81%, 1.54%, and 1.96%, respectively, which satisfy the requirement of EVM in the 3GPP standard [9] within 8%. In the ACRR evaluation, 46.54dBc, 51.27dBc, and 42.40dBc are shown in the lower band, and 50.91dBc, 50.46dBc and 42.41dBc are in the upper band, respectively.

IV. Conclusion

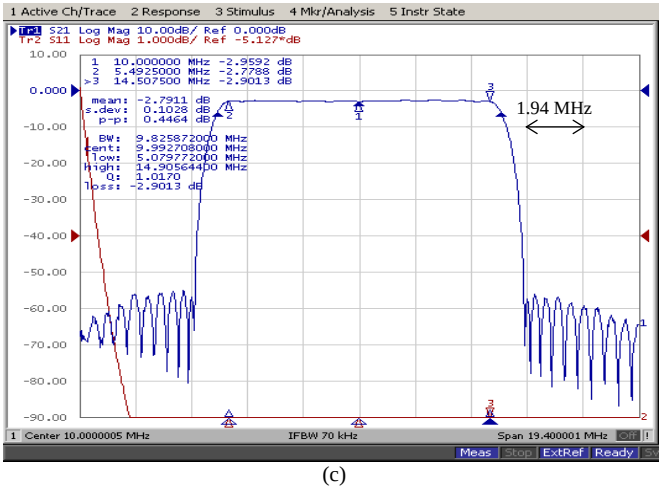
In this brief, we presented the reconfigurable digital IF filter with low complexity, which can adjust both the center frequency from 10MHz to 62.5MHz and the bandwidth among 10MHz, 15MHz, and 20MHz. These specifications were required in the mobile communication standards. The digital IF filter adopted a filter bank structure and a multi-stage scheme in order to reduce the hardware costs effectively while showing



(a)



(b)



(c)

Fig. 5. Frequency responses: (a) 62.5MHz of the center frequency and 20MHz of the bandwidth. (b) 42.5MHz of the center frequency and 20MHz of the bandwidth. (c) 10MHz of the center frequency and 10MHz of the bandwidth.

the same frequency selectivity as analogue SAW filter. The proposed digital IF filter not only satisfied the current standard of wireless communications but could be applied to changing mobile services by simply modifying the control software. The proposed system could also actively cope with sudden changes such as frequency re-allocation. It was expected that the proposed IF filter could minimize the system costs including exhaustive development caused by the frequent change of services and frequency policies.

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TABLE VI
PERFORMANCE SUMMARY AND COMPARISON

CENTER FREQUENCY 62.5 MHz/20 MHz BANDWIDTH						
		3GPP standard requirement [8]				Measurement
Parameter	Condition	Min.	Typ.	Max.	Unit	
Center Frequency	@3dB BW	62.35	62.5	62.65	MHz	62.43
Insertion Loss				10	dB	4.90
Inband					MHz	19.0
40dB Bandwidth				21.6	MHz	21.57
Amplitude Ripple				-	dB	1.36
Group Delay					usec	1.55
EVM				8	%	1.81
ACRR	Lower	20			dBc	46.56
	Upper					50.91
CENTER FREQUENCY 42.5 MHz/20 MHz BANDWIDTH						
		3GPP standard requirement [8]				Measurement
Parameter	Condition	Min.	Typ.	Max.	Unit	
Center Frequency	@3dB BW	42.35	42.5	42.65	MHz	42.45
Insertion Loss				10	dB	3.56
Inband					MHz	19.0
40dB Bandwidth				21.6	MHz	21.39
Amplitude Ripple				-	dB	0.89
Group Delay					usec	1.45
EVM				8	%	1.54
ACRR	Lower	20			dBc	51.27
	Upper					50.46
CENTER FREQUENCY 10.0 MHz/10 MHz BANDWIDTH						
		3GPP standard requirement [8]				Measurement
Parameter	Condition	Min.	Typ.	Max.	Unit	
Center Frequency	@3dB BW	9.85	10.0	10.15	MHz	10.01
Insertion Loss				10	dB	2.79
Inband					MHz	9.0
40dB Bandwidth				11.6	MHz	11.29
Amplitude Ripple				-	dB	0.48
Group Delay					usec	1.78
EVM				8	%	1.96
ACRR	Lower	20			dBc	42.40
	Upper					42.41