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High Step-Up PWM DC-DC Converter with Coupled-Inductor and Resonant Switched-Capacitor

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***Abstract*—In this paper, a novel high step-up PWM DC-DC converter integrating coupled-inductor and switched-capacitor (SC) techniques is presented. The proposed converter consists of a synchronous rectification Boost unit and multiple coupled-inductor-SC (CLSC) units. Its structure can therefore be easily extended for ultra-high voltage gain. The diodes employed in the proposed converter can operate under soft-switching condition by utilizing leakage inductance of the coupled inductor. Low-voltage-rated transistors can be used to improve the efficiency as the voltage stress on the main switches of the proposed converter is reduced. The feasibility of the proposed converter is experimentally demonstrated by a 200W prototype converter.**

***Index Terms*—DC-DC converter, coupled-inductor, switched-capacitor, soft-switching.**

I. Introduction

VARIOUS low DC voltage sources and energy storage devices, like photovoltaic (PV) cells, fuel cells, battery and supercapacitor, are usually need to be boosted to a high AC voltage level for industrial applications [1]. One solution is to use step-up multilevel inverters to convert them to a high AC voltage directly [2]. Another mean is to employ high step-up DC-DC converters to first boost them to a high DC level and then to connect with a full bridge [3].

For high step-up DC-DC conversion, transformer-based switched-mode power supplies (SMPSs), like Flyback and Forward converters etc., are normally applied due to their simple structure. In recent years, many novel high step-up DC-DC converters have been developed by utilizing one or several of the following techniques: switched-capacitor (SC) also known as voltage-multiplier or charge pump, switched-inductor, tapped-inductor and coupled-inductor. For instance, high step-up zero-current switching (ZCS) converters implemented by resonant SC technique are presented in [4]-[7]. A high step-up converter and a step-down version integrating Buck/Boost and SC techniques are presented in [8] and [9], respectively. The literature [10] proposes a high step-up converter based on switched-inductor structure. With the combination of SC and switched-inductor techniques, a series of single-stage switched-capacitor-inductor converters is introduced in [11]. One type of high step-up converters based on tapped-inductor is introduced in [12] and another type based on coupled-inductor is presented in [13] and [14].

Among these new techniques, the combination of coupled-inductor and SC is most widely adapted for high voltage gain. Specifically, multiple novel high step-up converters based on coupled-inductor and SC structure are introduced in literatures [15]-[26]. Their common features are that the voltage conversion ratio can be regulated in PWM mode; less active switches and magnetic components are employed. For instance, only one active switch and one coupled inductor are employed in the converters of [15], [16], [17], [19], [20] to implement high voltage conversion ratio. Even for the interleave structures proposed in [18], [22] and [25], there are just two active switches and two coupled inductors. This feature makes this type of converters is superior in the respects of cost and size.

In this paper, the combination concept of coupled-inductor and SC is further developed for a novel high step-up DC-DC converter. The structure of the proposed converter can be easily extended for ultra-high voltage gain. With resonant SC technique, diodes employed in the proposed converter can operate under ZCS condition. Different from those resonant SC converters proposed in [4]-[7], the proposed converter utilizes leakage inductance of the coupled inductor, rather than an additional resonant inductor, to implement resonance. Simulation and experimental results are provided to demonstrate the effectiveness of the proposed high step-up converter.

II. Proposed Step-Up DC-DC Converter

The circuit configuration of the proposed high step-up converter is shown in Fig.1. It comprises a synchronous rectification Boost unit and multiple coupled-inductor-SC (CLSC) units. Only one magnetic component, i.e. a coupled inductor, is employed in the proposed converter. Each CLSC unit includes two capacitors C_i and C_{Si}, two diodes D_{i1} and D_{i2}, as well as one winding having n_i turns of the coupled inductor,

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here i ranges from 2 to m. The synchronous rectification Boost unit is made up of a DC input voltage source V_{in}, a pair of complementary conduction transistors S_1 and S_2, a filter capacitor C_1 and the primary side winding with n_1 turns of the coupled-inductor. Filter capacitors C_1 to C_m are connected in series with the input voltage source to provide the total voltage for load. To facilitate the derivation of the ideal voltage conversion ratio, two assumptions are made as: all components including the input voltage source V_{in} are ideal; all capacitors are so large that their voltages can be seen as constant.

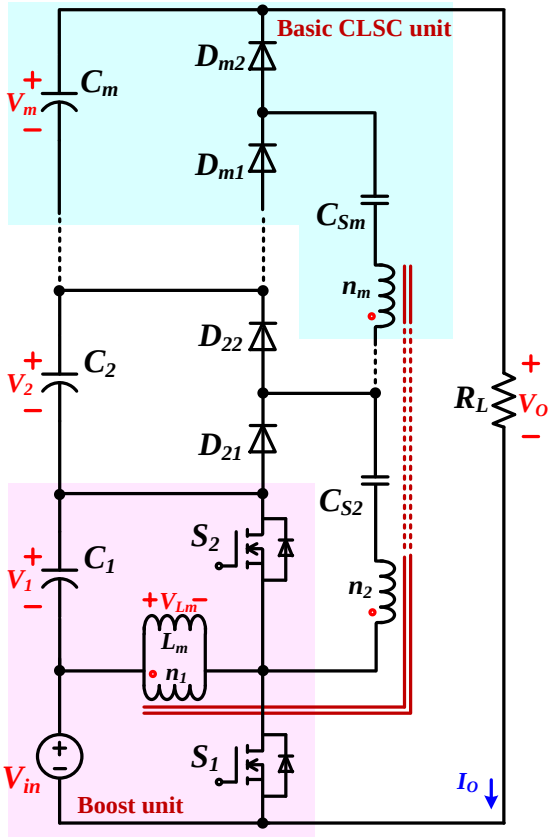


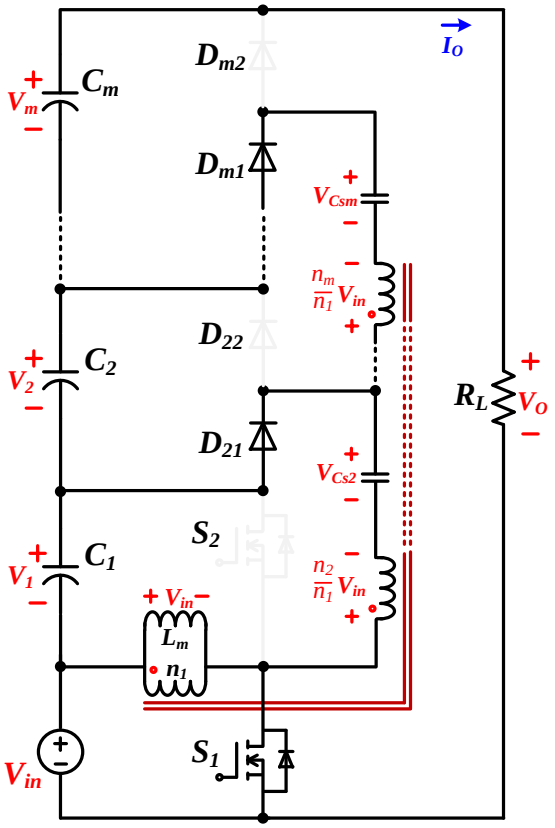
Fig.1. The proposed high step-up converter.

As the two transistors operate in complementary manner, the operation of the proposed converter can be simplified to two states as shown in Fig.2. When the transistor S_1 is turned ON while S_2 is OFF, the state circuit is shown in Fig.2(a). Based on the assumption made before, the state circuit can be mathematically described as

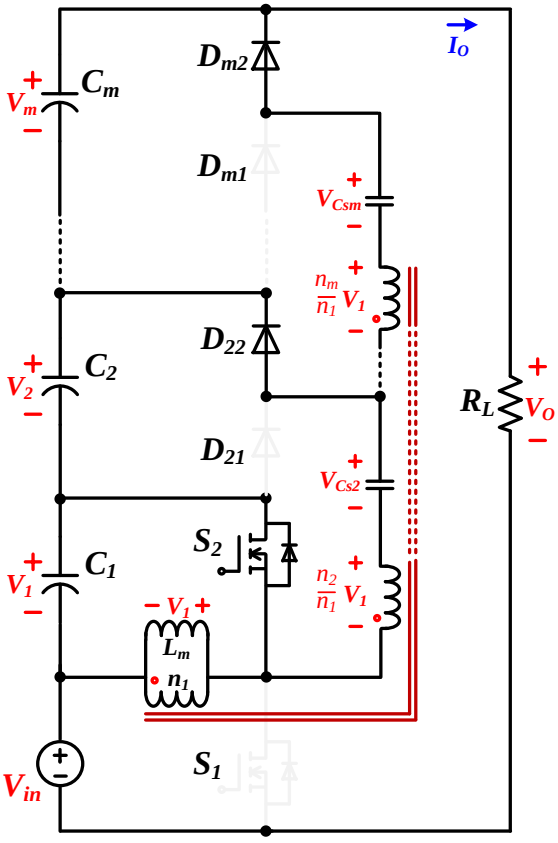
$$\begin{cases} V_{C_{S2}} = V_{in} + V_1 + \dfrac{n_2}{n_1} V_{in} \\ V_{C_{Si}} = V_{i-1} + \dfrac{n_i}{n_1} V_{in} \quad ,i = 3,....,m \end{cases} \tag{1}$$

When the transistor S_1 is turned OFF while S_2 is ON, the state circuit is shown in Fig. 2(b). Similarly, the state circuit can be also mathematically described as

$$V_i = V_{C_{Si}} + \frac{n_i}{n_1} V_1 \quad ,i = 2,....,m \tag{2}$$



(a)



(b)

Fig.2. Two state circuits of the proposed converter. (a) S_1 ON and S_2 OFF. (a) S_1 OFF and S_2 ON.

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Applying volt-second balance on the magnetizing inductance L_m and combing the two expressions (1) and (2), the capacitor voltages V_1 to V_m and V_{CS2} to V_{CSm} can be derived and are expressed as

$$V_{C_{Si}} = \left(\frac{1}{1-d}\sum_{k=1}^{i-1}\frac{n_k}{n_1}+\frac{n_i}{n_1}\right)V_{in} \quad ,i=2,....,m \tag{3}$$

$$\begin{cases} V_1 = \dfrac{d}{1-d}V_{in} \\ V_i = \dfrac{V_{in}}{1-d}\sum_{k=1}^{i}\dfrac{n_k}{n_1} \quad ,i=2,....,m \end{cases} \tag{4}$$

where d is the duty ratio of the transistor S_1.

The output voltage of the converter is the sum of V_1 to V_m as well as the input voltage V_{in}, i.e.

$$V_O = V_{in} + \sum_{k=1}^{m} V_k \tag{5}$$

Substituting (4) into (5), the output voltage V_O can be further expressed as

$$V_O = V_{in} + \frac{d}{1-d}V_{in} + \sum_{k=2}^{m}\left(\frac{V_{in}}{1-d}\sum_{i=1}^{k}\frac{n_i}{n_1}\right) = \frac{V_{in}}{1-d}\sum_{k=1}^{m}\frac{n_k}{n_1}(m+1-k) \tag{6}$$

As a result, the ideal voltage conversion ratio of the proposed converter can be derived from (6) and is given as

$$\frac{V_O}{V_{in}} = \frac{1}{1-d}\sum_{k=1}^{m}\frac{n_k}{n_1}(m+1-k) \tag{7}$$

where again the number of CLSC units employed in the propose converter is *m-1*; and n_k/n_1, $k=2,...,m$, is the turns ratio of the coupled-inductor. For the two special cases when there are the same turns $n_1=n_2=...=n_m$ for all windings, and when there is the same turns ratio $n=n_2/n_1=...=n_m/n_1$ for the coupled-inductor, the voltage conversion ratio can be simplified as

$$\left.\frac{V_O}{V_{in}}\right|_{n_1=n_2=...=n_m} = \frac{m(m+1)}{2(1-d)} \tag{8}$$

$$\left.\frac{V_O}{V_{in}}\right|_{n=\frac{n_2}{n_1}=...=\frac{n_m}{n_1}} = \frac{nm(m-1)+2m}{2(1-d)} \tag{9}$$

Fig.3 illustrates the variations of the ideal voltage gain versus the duty cycle of the transistor S_1 with different turn's ratios of the coupled inductor. It intuitively indicates that the proposed converter is capable of providing ultra-high voltage conversion ratio by employing multiple CLSC units or setting a larger turn's ratio of the coupled inductor or increasing the duty ratio. For a specific converter, the turn's ratio and the number of CLSC units are fixed, output voltage is controlled by changing the duty ratio in PWM mode to withstand the load and input voltage fluctuations. Similar to conventional SMPCs, the duty ratio of the proposed converter cannot be too great and it is usually below 0.8. The turn's ratio is usually not less than 1 for step-up applications. However, it is impossible to get a too larger turn's ratio for the coupled inductor in practice. The number of CLSC units can be determined by (8) when n=1 or (9) when n>1. For instance, the duty ratio is set to 0.5 and the turn's ratio is 2, and then the value m of a converter converting 24V to 200V is calculated as 2.

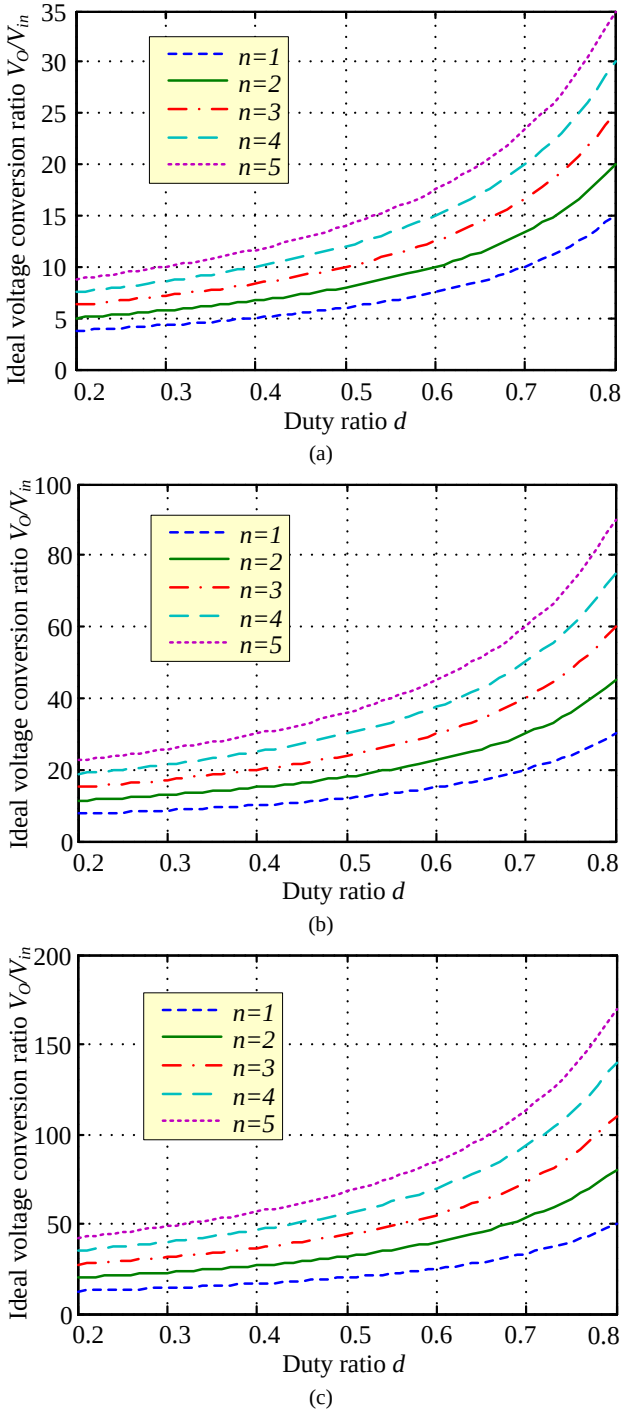

Fig.3. Voltage gain versus duty cycle under various turns ratios. (a) With one CLSC unit. (b) With two CLSC units. (c) With three CLSC units.

III. Steady Analysis with Leakage Inductances and Parasitic Resistances

Based on the assumptions that 1) the primary side winding of the coupled inductor is ideal, i.e. no leakage inductance and parasitic resistance, and 2) the input voltage source V_{in} is ideal, i.e. constant and no series impedance, the proposed converter with one CLSC unit, i.e. $m=2$, is shown in Fig.4, wherein L_k is

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the leakage inductance of the secondary side winding of the coupled-inductor and R is the total parasitic resistance of the components including one transistor $S_{1,2}$, one diode $D_{1,2}$, one capacitor $C_{1,2}$ and the secondary side winding of the couple inductor.

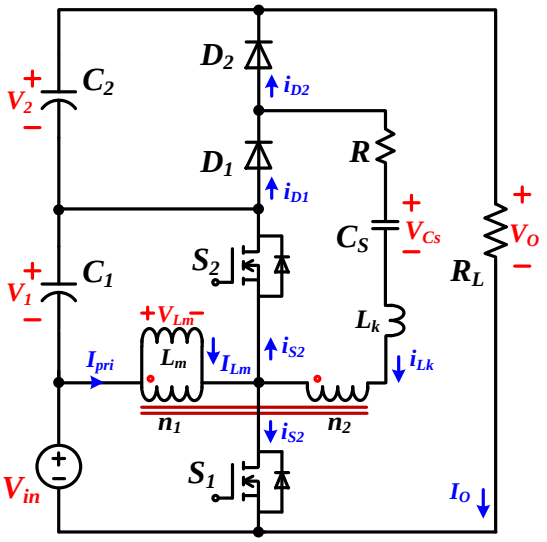

Fig.4. Circuit configuration of the proposed converter with soft-switching.

A. State Analysis

As mentioned before, transistors S_1 and S_2 operate in a complementary manner. Based on the assumption that the Q factor of the R-L_k-C_S tank is greater than 0.5, i.e. $Q=\sqrt{L_k/C_S}/R>0.5$, there are four working states in one period of switching cycle. Fig. 5 shows the four state circuits and the corresponding idealized waveforms are illustrated in Fig. 6, wherein $i_{S1,2}$ and $i_{D1,2}$ are the current flowing through the two transistors and the two diodes; I_{Lm} and I_{pri} are the excitation current and the current flowing through the primary side winding of the coupled inductor, respectively; i_{Lk} is the current flowing through the R-L_k-C_S tank as well as the secondary side winding of the couple inductor; V_F is the forward voltage drop of the diode $D_{1,2}$ and n is the turns ratio of the coupled inductor, i.e. $n=n_2/n_1$. The capacitors C_1 and C_2 are assumed to be far larger than C_S and both of their voltages V_1 and V_2 can be seen as constant.

State I [t_0<t<t_1 see Fig. 5(a)]: This state starts by turning S_1 ON while S_2 OFF. The input voltage V_{in} is directly across the primary side winding of the coupled inductor so that the excitation current I_{Lm} rises linearly from its minimum value I_{min}. At the same time, a higher voltage $(n+1)V_{in}+V_1-V_F$ is developed across the R-L_k-C_S tank resulting in the resonant current i_{Lk} increases from zero in underdamping resonant mode. The diode D_1 is therefore turned ON under ZCS and this state can be also mathematically described as

$$\begin{cases} i_{Lk}(t)=\dfrac{(n+1)V_{in}+V_1-V_F-V_{C\min}}{\omega_r L_k}e^{-\beta(t-t_0)}\sin\omega_r(t-t_0) \\ V_{Cs}(t)=V_{C\min}+\dfrac{1}{C_S}\int_{t_0}^{t} i_{Lk}(\tau)d\tau \end{cases} \tag{10}$$

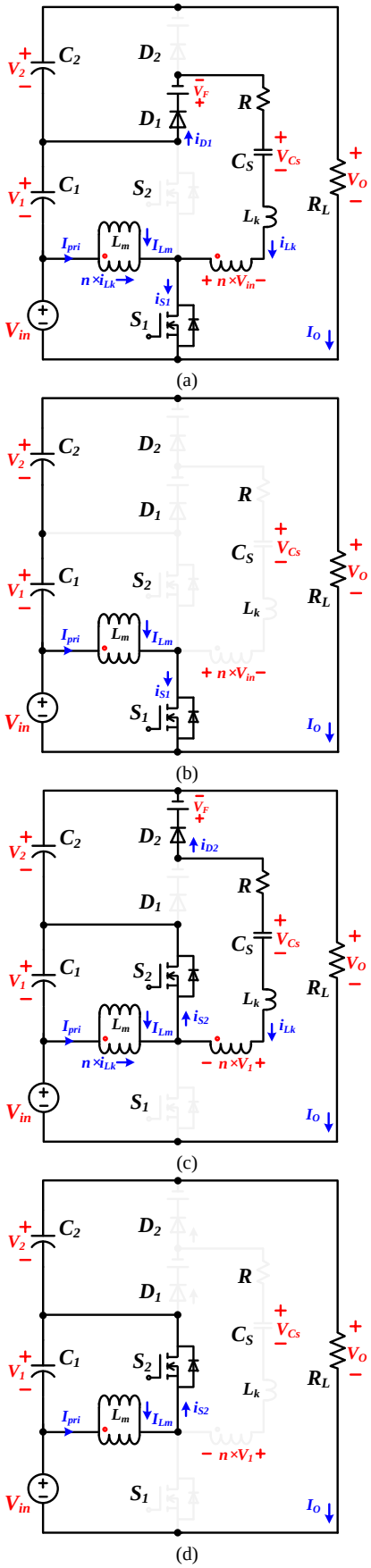

Fig.5. Operation state circuits. (a) State I. (b) State II. (c) State III. (d) State IV.

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$$\begin{cases} I_{Lm}(t) = I_{\min} + \dfrac{V_{in}}{L_m}(t-t_0) \\ I_{pri}(t) = I_{Lm}(t) + n \times i_{Lk}(t) \\ i_{S1}(t) = I_{Lm}(t) + (n+1) \times i_{Lk}(t) \\ i_{D1}(t) = i_{Lk}(t) \end{cases} \quad (11)$$

where V_{Cmin} is the initial voltage across the capacitor C_S.

State II [t_1<t<t_2 see Fig. 5(b)]: Based on the assumption that the conduction duration of the transistor S_1 is longer than half of a period of the resonant frequency, i.e. $d \times T_S \geq \pi/\omega_r$, here T_S is the switching cycle, $\omega_r = \sqrt{1/(L_k C_S) - \beta^2}$ is the damped resonant angular frequency and $\beta = R/(2L_k)$, the resonant current i_{Lk} changes back to zero after half a period of the resonant frequency, and the diode D_1 is therefore OFF naturally. The capacitor voltage V_{Cs} reaches to its maximum value V_{Cmax} and this value will be maintained until the next operation state. The excitation current continues to increase linearly and this state is mathematically described as

$$V_{C\max} = (n+1)V_{in} + V_1 - V_F + [(n+1)V_{in} + V_1 - V_F - V_{C\min}]e^{-\beta\pi/\omega_r} \quad (12)$$

$$i_{S1}(t) = I_{pri}(t) = I_{Lm}(t) = I_{\min} + \frac{V_{in}}{L_m}(t-t_0) \quad (13)$$

At the end of this state, the excitation current reaches to its maximum value I_{max}, i.e.

$$I_{\max} = I_{\min} + \frac{V_{in}}{L_m} dT_S \quad (14)$$

where again d is the duty ratio of the transistor S_1 and T_S is the switching cycle.

State III [t_2<t<t_3 see Fig. 5(c)]: This state starts by turning S_1 OFF while S_2 ON. The capacitor voltage V_1 is inversely across the primary side winding of the coupled inductor resulting in the excitation current I_{Lm} falls linearly from its maximum value I_{max}. At the same time, a lower voltage $V_2+V_F-nV_1$ is developed across the R-L_k-C_S tank so that the resonant current i_{Lk} increases from zero in reverse direction. The diode D_2 is therefore turned ON under ZCS and this state can be mathematically described as

$$\begin{cases} i_{Lk}(t) = \dfrac{V_2 + V_F - nV_1 - V_{C\max}}{\omega_r L_k} e^{-\beta(t-t_2)} \sin \omega_r (t-t_2) \\ V_{Cs}(t) = V_{C\max} + \dfrac{1}{C_S}\int_{t_2}^{t} i_{Lk}(\tau) d\tau \end{cases} \quad (15)$$

$$\begin{cases} I_{Lm}(t) = I_{\max} - \dfrac{V_1}{L_m}(t-t_2) \\ I_{pri}(t) = I_{Lm}(t) + n \times i_{Lk}(t) \\ i_{S2}(t) = I_{Lm}(t) + (n+1) \times i_{Lk}(t) \\ i_{D2}(t) = -i_{Lk}(t) \end{cases} \quad (16)$$

State IV [t_3<t<t_4 see Fig. 5(d)]: Based on the assumption that the conduction duration of the transistor S_2 is longer than half of a period of the resonant frequency, i.e. $(1\text{-}d) \times T_S \geq \pi/\omega_r$, the resonant current i_{Lk} changes back to zero again after half a period of the resonant frequency, and the diode D_2 is OFF naturally. The capacitor voltage V_{Cs} reaches to its minimum value V_{Cmin} and this value will be maintained until when the transistor S_1 is turned ON while S_2 is OFF. During this stage, the excitation current continues to decrease linearly. And this state is mathematically described as

$$V_{C\min} = V_2 + V_F - nV_1 - [V_{C\max} - (V_2 + V_F - nV_1)]e^{-\beta\pi/\omega_r} \quad (17)$$

$$i_{S2}(t) = I_{pri}(t) = I_{Lm}(t) = I_{\max} - \frac{V_1}{L_m}(t-t_2) \quad (18)$$

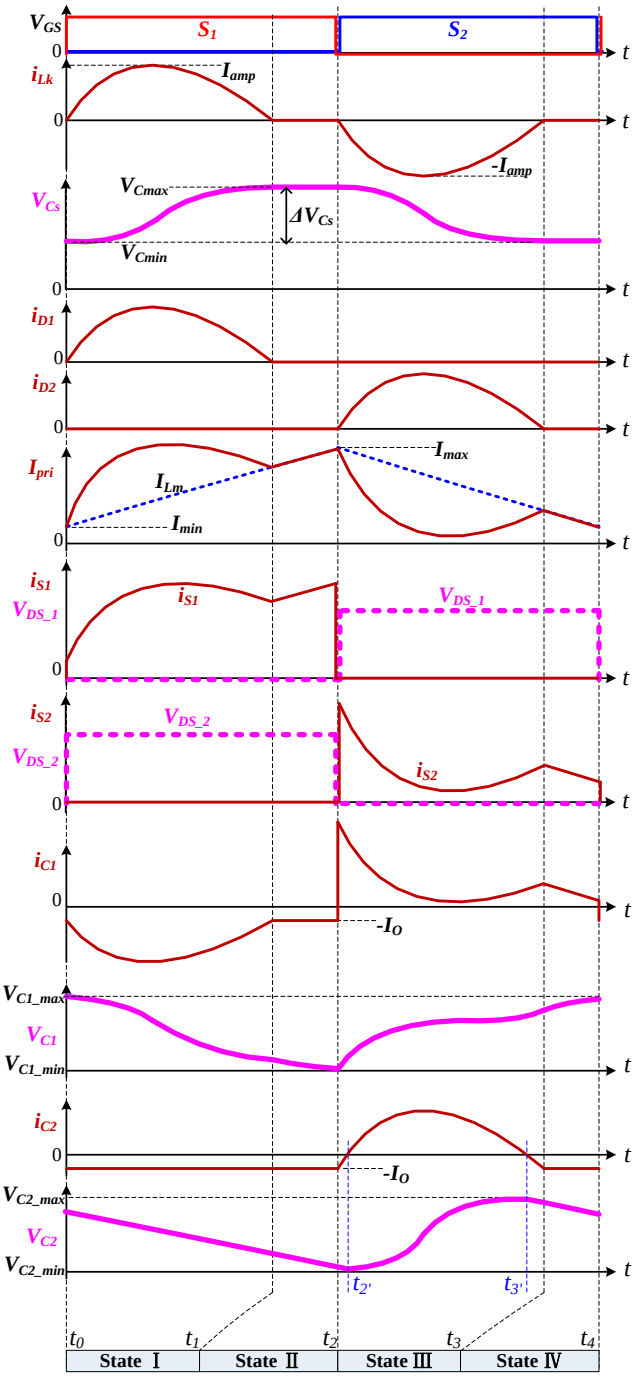

Fig.6. Idealized waveforms of the proposed soft-switching converter.

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B. Analysis and Comparison on Voltage Transfer Gain

The voltage ripple of the capacitor C_S is derived by (12)-(17), i.e.

$$\Delta V_{Cs} = V_{C\max} - V_{C\min} = [(n+1)(V_{in}+V_1) - V_2 - 2V_F]\frac{1+e^{-\beta\pi/\omega_r}}{1-e^{-\beta\pi/\omega_r}} \tag{19}$$

Applying the volt-second balance principle on the magnetizing inductance L_m, the capacitor voltages V_1 and V_2 can be derived from (19) and are given as

$$\begin{cases} V_1 = \dfrac{d}{1-d}V_{in} \\ V_2 = \dfrac{n+1}{1-d}V_{in} - 2V_F - \Delta V_{Cs}\dfrac{1-e^{-\beta\pi/\omega_r}}{1+e^{-\beta\pi/\omega_r}} \end{cases} \tag{20}$$

The charge balance principle of the capacitor C_S is described as that the amount of charge flowing into/out of the capacitor is the same as that flowing through the load during one switching cycle, i.e. $C_S \times \Delta V_{Cs} = I_O \times T_S$. Hence, the actual output voltage $V_O = V_1 + V_1 + V_2$ of the converter is derived from (20), i.e.

$$V_O = \frac{n+2}{1-d}V_{in} - 2V_F - \frac{1}{C_S f_S}\tanh\left(\frac{\pi}{2\sqrt{4Q^2-1}}\right) \times I_O \tag{21}$$

where gain f_S is the switching frequency of the converter. It indicates that the forward voltage drop $2V_F$ of the two diodes is directly reflected on the output voltage drop. And the influence of the R-L_k-C_S resonant tank is equivalent to an output impedance which is a function of the switching frequency f_S, the capacitance C_S and the Q factor.

When all components are ideal, the voltage gain is $V_O/V_{in} = (n+2)/(1-d)$. The comparison works, with existing converters based on switched-capacitor and dual-winding coupled-inductor, are given in Table I. It indicates that a higher voltage transfer gain is usually achieved by employing more capacitors and switching devices including transistors and diodes. Although the proposed converter has not the highest gain, it has advantages of simple structure and easy expansion. Higher voltage transfer gains can be achieved by employing multiple CLSC units as analyzed in the previous section.

TABLE I
COMPARISON WITH EXISTING HIGH STEP-UP CONVERTERS

Converters	Voltage gain V_O/V_{in}	Number of capacitors	Number of switches
[26]	$\dfrac{2+n-d}{1-d}$	2	3
Proposed	$\dfrac{2+n}{1-d}$	3	4
[16]	$\dfrac{1+n+nd}{1-d}$	4	5
[15]	$\dfrac{2+n+nd}{1-d}$	4	5
[20]	$\dfrac{1+2n+nd}{1-d}$	6	7

C. Design of Capacitors and Coupled-Inductor

Selection of capacitor employed in the proposed converter is based on two factors: 1) capacitors' voltage stresses which have been analyzed before and; 2) ripple in the capacitor voltages. During both states I and II, the filter capacitor C_1 discharges causing its voltage falls from V_{C1_max} to V_{C1_min} as shown in Fig.6. The capacitance can therefore be expressed as a function of the voltage ripple, i.e.

$$C_1 = \frac{1}{\Delta V_{C1}}\left[\int_{t_0}^{t_1} i_{D1}(t)dt + \int_{t_0}^{t_2} I_O dt\right] = \frac{(1+d)I_O}{\Delta V_{C1} f_S} \tag{22}$$

where $f_S = 1/T_S$ is the switching frequency; ΔV_{C1} is the voltage ripple across C_1 and it should be as small as possible to reduce the output voltage ripple.

For the filter capacitor C_2, it is charged by a current (i_{D2}-I_O) from the moment $t_{2'}$ to $t_{3'}$, as shown in Fig.6, making its voltage rises from V_{C2_min} to V_{C2_max}. Its voltage ripple is thus equal to the integral of the charging current divided by its capacitance. As the periods (t_2 - t_2) and (t_3 - $t_{3'}$) are very short, the capacitance C_2 can be approximately estimated by the following expression

$$C_2 \approx \frac{1}{\Delta V_{C2}}\left[\int_{t_0}^{t_2} I_O dt + \int_{t_3}^{t_4} I_O dt\right] = \frac{I_O}{\Delta V_{C2} f_S}\left(1 - \frac{f_S}{2f_r}\right) \tag{23}$$

where $f_r = \omega_r/(2\pi)$ is the resonant frequency; ΔV_{C2} is the voltage ripple across C_2 and it also should be as small as possible to reduce the output voltage ripple.

During one switching cycle, charge flowing through the load is totally transferred by the switched capacitor C_S. The capacitance C_S can therefore be determined by

$$C_S = \frac{I_O}{\Delta V_{Cs} f_S} \tag{24}$$

where I_O is the output current; ΔV_{Cs} is the voltage ripple across C_S. It should be noted that the value $\Delta V_{Cs}/2$ must be smaller than the DC-bias voltage $V_{in} \times [n+1/(1-d)]$ across the capacitor C_S.

The value of the leakage inductance L_k can be estimated by the resonant frequency f_r and the value of the capacitance C_S, i.e.

$$L_k \approx \frac{1}{(2\pi f_r)^2 C_S} \tag{25}$$

Design of the magnetizing inductance L_m is based on two factors: one is the current ripple $(V_{in}/L_m) \times dT_S$, and another is winding turns. Larger value of L_m means smaller current ripple but requires more turns of winding and this will also cause more leakage inductance on the primary side, and vice versa. Hence the two items of current ripple and coil turns should be considered comprehensively. As the converter is proposed for high step-up applications, the turns ratio $n = n_2/n_1$ should be greater than 1. The leakage inductance on the secondary side is therefore larger than that on the primary side. Moreover, to reduce the leakage inductance, a couple-inductor with sandwich coils or pie winding structure is recommended for the proposed converter.

D. Voltage and Current Stresses of Switches

Switch selection is mainly based on voltage and current stresses. For the proposed converter, voltage stresses on the transistors $S_{1,2}$ are the same, and are given by

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$$V_{DS\_1,2} = V_{in} + V_1 = \frac{V_{in}}{1-d} \tag{26}$$

Voltage stresses on the diodes $D_{1,2}$ are also the same, and are given by

$$V_{D1,2} = V_2 = \frac{n+1}{1-d} V_{in} \tag{27}$$

When the parasitic resistance R is so small that can be ignored, the resonant current i_{Lk} will change in a sinusoidal manner, i.e. $i_{Lk}(t) = I_m \sin(\omega_r' t)$, here $\omega_r' = 1/\sqrt{L_k C_S}$ is the undammed resonant angular frequency and I_m is the amplitude of the resonant current. By applying charge balancing on the switched capacitor C_S, the average values and maximum values of the diode currents can be derived as

$$\begin{cases} I_{av\_D1,2} = \dfrac{1}{T_S}\int_0^{T_S} i_{D1,2}(t)dt = I_O \\ I_{\max\_D1,2} = \pi \dfrac{f_r}{f_S} I_O \end{cases} \tag{28}$$

Furthermore, RMS values of the transistors $S_{1,2}$ can be universally given by

$$I_{S1,2(rms)} \approx \sqrt{a \times I_O^2 + b \times (\frac{V_{in}}{f_S L_m}) I_O + c \times (\frac{V_{in}}{f_S L_m})^2} \tag{29}$$

where the three coefficients a, b and c are determined by circuit parameters and their specific expression are given as

For S_1:

$$\begin{cases} a = \dfrac{\pi^2 f_r}{4 f_S} + \dfrac{(n+3)(3+dn)}{(1-d)^2} \\ b = \dfrac{f_S}{2 f_r} - \dfrac{3d}{2} \\ c = \dfrac{d^3}{12} \end{cases} \tag{30}$$

For S_2:

$$\begin{cases} a = \dfrac{\pi^2 f_r}{4 f_S} + \dfrac{(n+3)(n+2)}{1-d} \\ b = \dfrac{d f_S}{2(1-d) f_r} - \dfrac{3d}{2} \\ c = \dfrac{d^2(1-d)}{12} \end{cases} \tag{31}$$

IV. Simulation and Experimental Verifications

A. Simulation Results

To verify the feasibility of the proposed high step-up converter shown in Fig.1, simulation models with different numbers of CLSC units (m=2, 3, 4) and different turn's ratios (n=1, 2, 3) have been built by PSIM and the simulation parameters are given as follows: V_{in}=24V; f_S=100 kHz; d=0.5; all switch devices are ideal; all filter capacitors C_1=C_2=C_3=C_4=100μF; all switched capacitors C_{S2}=C_{S3}=C_{S4}= 2.2μF; the magnetizing inductance of the coupled inductor is L_m=50μH; and the load is R_L=500Ω.

Fig.7 illustrates the simulation results and it indicates that higher voltage transfer ratio can be achieved by either increasing the turn's ratio of the coupled inductor or adding more CLSC units. With more CLSC units and greater turn's ratio, the proposed converter can provide ultra-high voltage transfer ratio. This is consistent with the theoretical analysis given in Section II. Simulation results are slightly lower than the theoretical values calculated by (9) as there is a small voltage drop caused by switched capacitors whose specific effects have been discussed in [28].

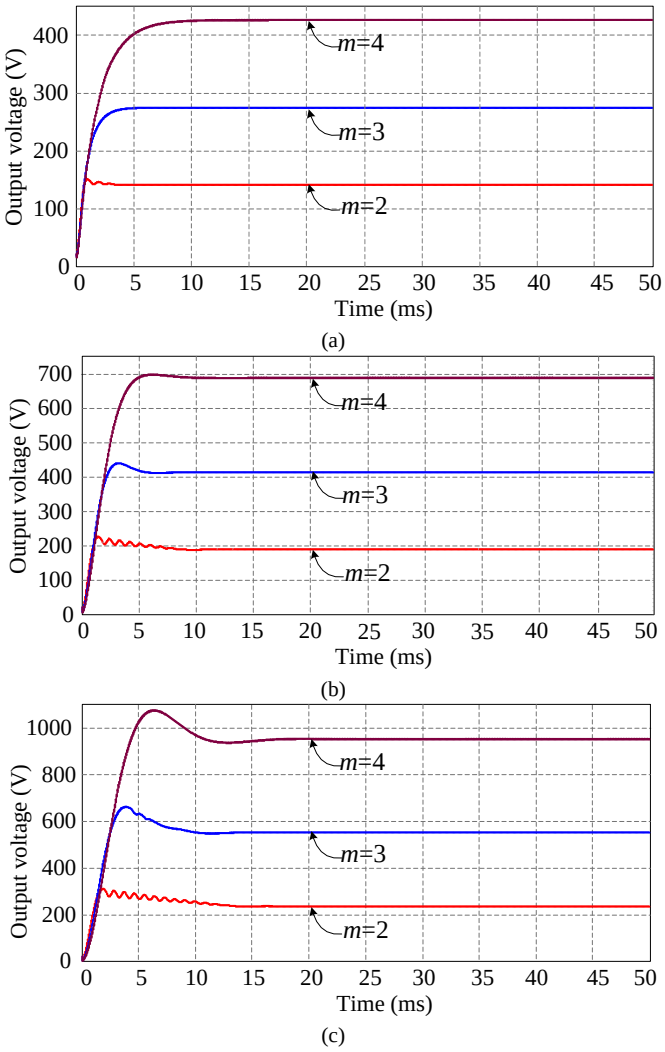

Fig.7. Simulation results of the proposed converter of Fig.1 with different numbers of CLSC units and different turn's ratios. (a) The turn's ratio n=1. (b) The turn's ratio n=2. (c) The turn's ratio n=3.

B. Experimental Results

To experimentally demonstrate the feasibility of the proposed converter, a 200W prototype circuit was built in laboratory by referring the circuit configuration of Fig.4 and the design considerations given in Sections III-C and III-D. Specifications and photograph of the prototype are given in Table II and Fig.8, respectively. The Q factor of the resonant tank in the prototype is about 13 and the resonant frequency is 78 kHz. Substituting the circuit parameters into (21), the voltage transfer relationship of the prototype converter is expressed as

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$$V_O = \frac{4.08}{1-d} V_{in} - 1.8 - 0.55 \times I_O \qquad (32)$$

Fig.9 illustrates the measured output voltage versus the output current when the input voltage is fixed at 24V. As the output current increases, the measured voltage drop rate is higher than the calculated result of (32). The main reason is that switching losses of S_1, S_2, magnetic losses of the coupled inductor and conduction losses in C_1, C_2 and C_{in} are not included in (32). However, the measured output voltage is very close to the calculated value when the output current is very low, e.g. 0.2A.

TABLE II
SPECIFICATION AND COMPONENTS OF THE 200W PROTOTYPE

Switching frequency f_S	50kHz
Input voltage V_{in} (Filter capacitor C_{in})	20~30VDC (180μF)
Capacitor C_1	180μF
Capacitor C_2	100μF
Coupled inductor n_1:n_2 (L_m; L_k)	12:25 (24.8μH; 1.9μH)
Switched capacitors C_S (ESR)	2.2μF (64mΩ)
S_1, S_2 [N-channel MOSFET] (on-state resistance)	IRFR3607PBF (7.34mΩ)
D_1, D_2 (Forward voltage drop V_F)	MUR820G (0.9V)

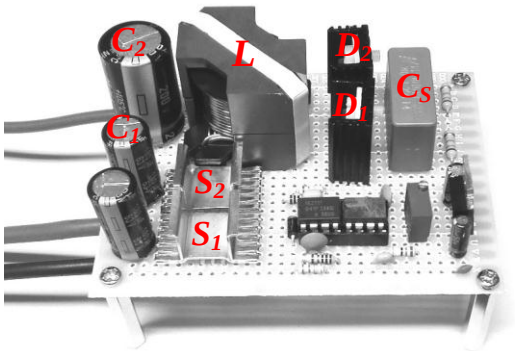


Fig.8. Hardware prototype of the proposed converter

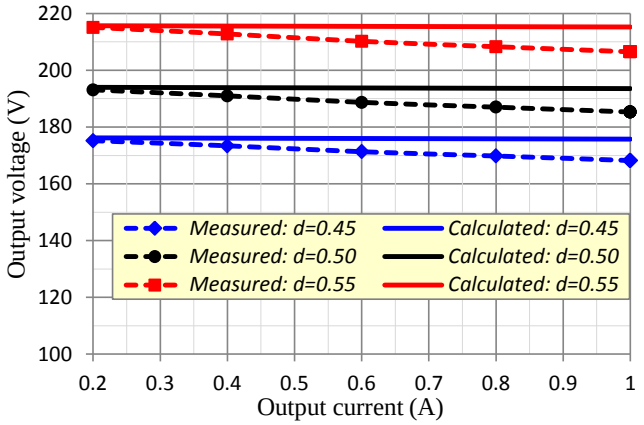
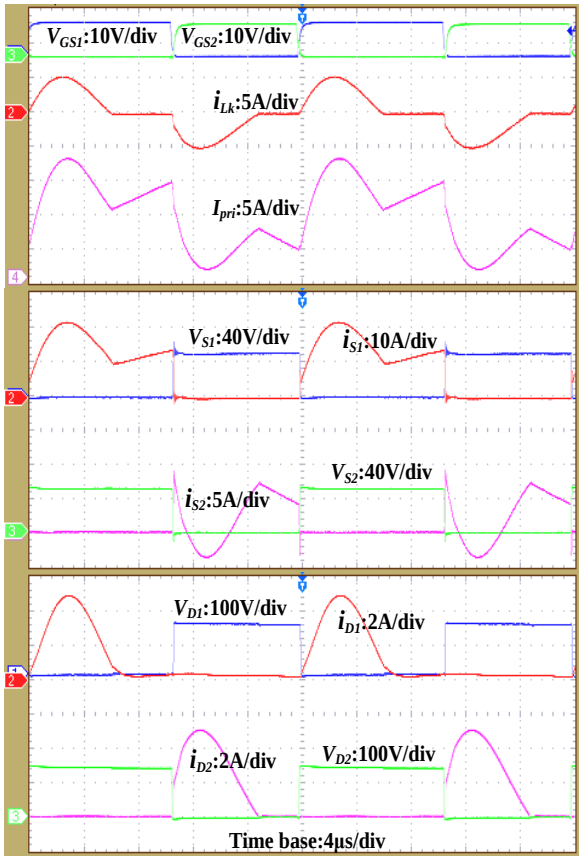
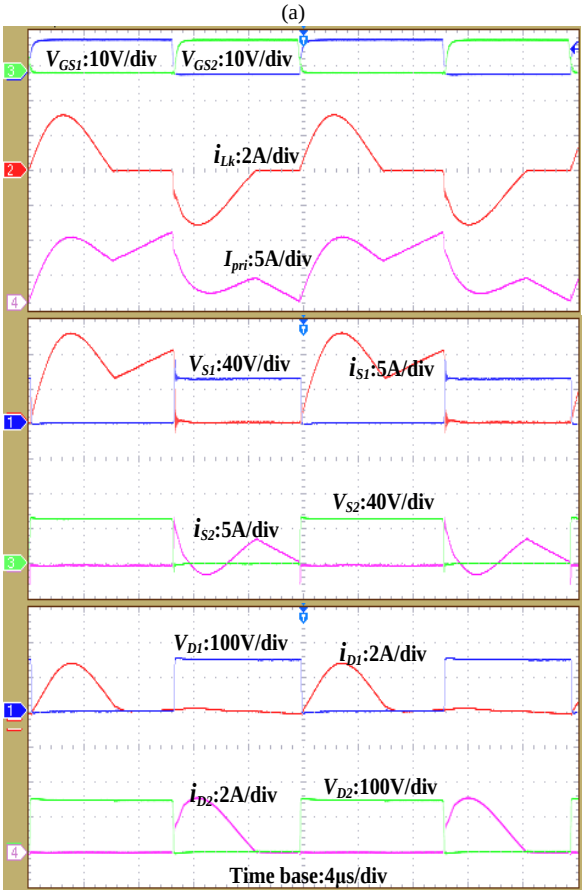


Fig.9. Measured output voltage versus output current when V_{in}=24V.



(a)



(b)

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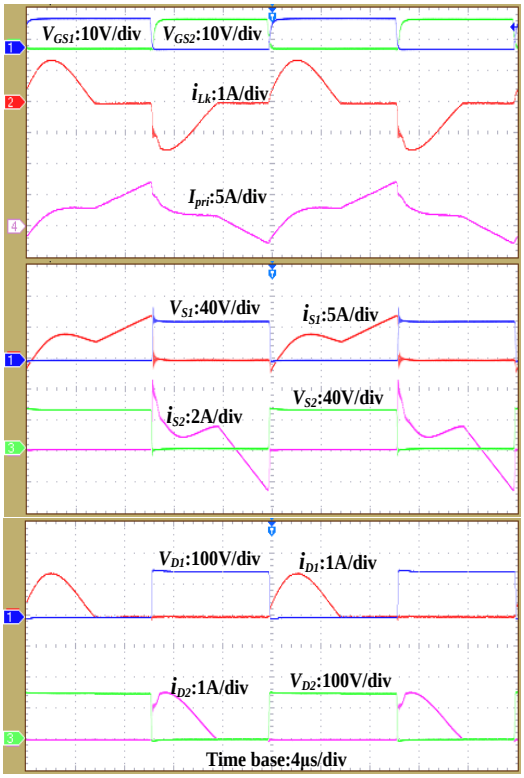

(c)

Fig.10. Experimental waveforms when V_{in}=24V and V_O=200V. (a) P_O=200W. (b) P_O=120W. (b) P_O=50W.

A simple voltage-type PI controller of the prototype is designed based on TL5001 [27]. Fig.10 shows the experimental waveforms when the input voltage is 24V, the output voltage is 200V and the output power is varied among 200W, 120W as well as 50W. The two transistors S_1, S_2 bear the same voltage stress about 50V. Low-voltage-rated MOSFETs with a small on-state resistance can therefore be used to improve the efficiency. With the resonant design, the two diodes D_1, D_2 operate under ZCS condition. With synchronous rectification achieved by S_1 and S_2, the excitation current will drop to below zero when the output power is lower than 120W, as shown in Fig.10(c). As a result, a part of energy charged in the capacitor C_1 will flow back to the input source and this will produce more conduction losses. One method to overcome this problem is to increase the magnetizing inductance L_m and another one is to avoid the converter operate under low power condition.

Fig.11 illustrates the prototype's efficiency which is the ratio of load power to the total input power. In addition to control and driver losses, the power loss of the prototype includes switching and conduction losses of transistors S_1 and S_2, the conduction loss caused by ESRs of capacitors C_1, C_2 and C_S, the conduction loss of diodes D_1 and D_2, the conduction loss caused by windings of the coupled-inductor, and magnetic losses. Along with the input voltage changes from 20V to 30V while the output voltage is fixed at 200V, the duty ratio of the converter increases from about 0.4 to 0.6. Within this range which is the recommended operating range, power loss caused by the change of the duty ratio is little. In contrast, a lower input voltage causes more conduction losses as the input current is higher. This is why there is a slightly higher efficiency in Fig.11 when the input voltage is higher. Overall, the efficiency can be higher than 91% when the output power varies from 60W to 200W. And the peak value of efficiency of the prototype is 93.9% which is achieved at P_O=120W and V_{in}=30V.

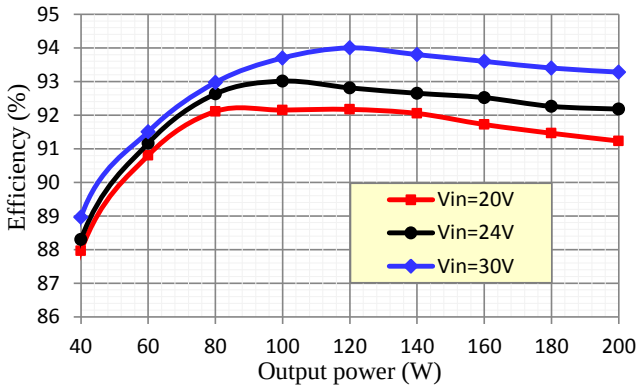

Fig.11. Measured efficiency versus output power when V_O=200V.

V. Conclusions

This paper presents a non-isolated high step-up DC-DC power converter implemented by the combination of coupled-inductor and switched-capacitor techniques. The proposed converter can be extended for ultra-high voltage gain by employing multiple CLSC units. The leakage inductance of the coupled inductor is utilized to achieve soft-switching of the diodes employed in the proposed converter. The voltage stress on the main switches is the same as that in the conventional Boost converter with the same input voltage and duty ratio. Hence, low-voltage-rated MOSFETs with small on-state resistance can be chosen to improve the efficiency. The feasibility of the proposed converter is experimentally verified by a 200W prototype which converts 24V to 200V.

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